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UNIVERSITY OF ALBERTA

REDUCTION OF WAITING TIME JITTER IN DIGITAL TDM SYSTEMS

BY

© QIONG ANGELA RUAN

A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES AND RESEARCH

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE

OF **MASTER OF SCIENCE**

DEPARTMENT OF ELECTRICAL ENGINEERING

EDMONTON, ALBERTA

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Date: 11th July 1991

DEDICATED TO

my husband and my parents

ABSTRACT

This study is concerned with the reduction of waiting time jitter in time division multiplexed digital communication systems. Waiting time jitter occurs when several lower rate digital signals are multiplexed to a higher data rate using pulse stuffing. Waiting time jitter is a low frequency timing noise impairment and, when present with large amplitudes, may degrade the performance of a network.

In this thesis, a new approach is described for reducing the waiting time jitter present on the recovered data for digital TDM systems. An improved desynchronizer is proposed, which makes use of the information (normally discarded) that is contained in the irregular stuff bit pattern. The new clock recovery circuit, named a *differential PLL* (DPLL), operates at the low frequency stuffing rate, so that very tight control of the recovered clock frequency can be obtained. Therefore, the waiting time jitter on the recovered digital signal can be reduced.

An experimental desynchronizer for a standard M12 multiplex system has been built. The peak-to-peak and the rms jitter of the recovered clock have been measured, and the jitter spectrum has been obtained. A peak-to-peak waiting time jitter of less than 0.2 unit intervals (UI), with an rms jitter value of less than 0.03 UI has been achieved over most of the DS-1 frequency range. The experimental results show that the waiting time jitter is reduced, as compared to the presently-used clock recovery method, by a factor of about 2.

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CHAPTER 1
INTRODUCTION

Just as there is a variety of analog transmission methods to accommodate signals of different bandwidths, likewise there are various digital facilities available in the digital hierarchy to permit the transmission of signals having different digital transmission rates. An important topic in telecommunications focuses on the interleaving of several different lower rate signals into a higher rate signal for transmission over a single channel, in order to make efficient use of an available higher speed facility. When a digital signal is multiplexed with other digital signals, a synchronization interface is required to feed the lower rate signals into the higher speed transmission system. Two necessary functions must be supplied at this synchronization interface: (1) extraction of an accurate timing signal, or clock signal, from the incoming signal, and (2) modifying the clock rate to make it compatible with the transmission system clock. These techniques have been discussed and investigated in the literature [1].

Timing accuracy is an important consideration in designing, developing and interconnecting digital systems and networks. Waiting time jitter, a type of low frequency clock impairment, is discussed in this thesis. Jitter is an impairment affecting digital signals in which individual signal elements are displaced from their ideal time positions. More formally, the CCITT definition is: "Jitter: Short-term variations of the significant instants of a digital signal from their ideal positions in time". Therefore, the timing impairment is often

termed *phase jitter*. As shown in Figure 1.1 [2], jitter can be represented as a continuous function of time.

The principal parameters that are of interest when considering the jitter performance in a digital transmission system are:

(1) Jitter generation: The amount of jitter the system produces on its own.

(2) Jitter transfer: The proportion of the input jitter that filters through to the output of the system.

(3) Jitter tolerance: The amount of jitter that can be tolerated at the input, before the system performance begins to deteriorate.

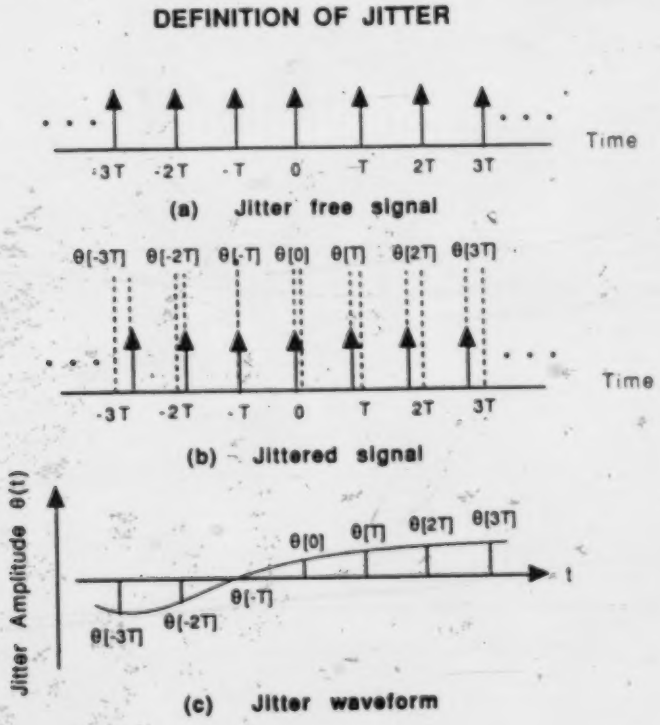


Figure 1.1 Illustration of jitter and its representation as a continuous time function.

The ability to reduce waiting time jitter is important for several reasons. When different bit rate signals are merged in a

telecommunication network, jitter accumulates and may degrade transmission performance. Due to the derived clock degradation, slips may be introduced into digital signals resulting from either data overflow or underflow from elastic stores. In addition, phase modulation of the reconstructed samples in digital-to-analog conversion devices may result in degradation of the digitally encoded signals. Because of its harmful effects on telecommunication systems, waiting time jitter needs to be controlled and kept within acceptable levels.

1.1 Thesis Objectives

The principal objective of this thesis is to investigate the possibility of reducing waiting time jitter in digital multiplex systems by improving the desynchronizer design. Specifically, a new desynchronizer for pulse-stuffed signals is proposed, which makes use of the much lower stuffing rate to control the digital phase-locked loop (PLL) clock recovery circuit.

The waiting time jitter reduction method which is proposed here can be used widely in digital multiplex systems employing pulse stuffing synchronization. Because of its relative simplicity and prior theoretical characterization, an M12 (DS-1 to DS-2) format has been used to describe and evaluate the new desynchronizer configuration. In this thesis, we limit the discussion to waiting time jitter and its reduction in M12 multiplex systems. To test the performance of the new desynchronizer, both a theoretical analysis and an experimental implementation are carried out. The waiting time jitter of the recovered clock is measured and compared with the presently-used

method. Also, the jitter spectrum is obtained, for frequency component analysis.

1.2 Thesis Organization

Chapter 1 introduces digital multiplex systems and describes jitter and the importance of controlling jitter in digital networks.

Chapter 2 describes the concepts of time division multiplexing and pulse stuffing synchronization. Waiting time jitter is formally defined, and its generation mechanism and its characteristics are briefly discussed.

Chapter 3 reviews the phase-locked loop (PLL) theory. Especially, the various types of digital PLL are discussed in more detail.

Chapter 4 describes a new approach for reducing waiting time jitter in TDM systems using an improved desynchronizer. Both theoretical analysis and experimental implementation are presented. The DPLL clock recovery circuit for the proposed desynchronizer in an M12 system is designed, and the important design parameters are measured and discussed.

Chapter 5 presents the experimental waiting time jitter results for the M12 system using the improved desynchronizer in the time domain and the frequency domain. The results indicate that the new desynchronizer (or clock recovery circuit) reduces the waiting time jitter by approximately 50% over most of input signal frequency range, as compared to the presently-used method.

Chapter 6 concludes the thesis. This chapter discusses the new desynchronizer system, and presents suggestions for possible future research directions in which additional work may proceed.

CHAPTER 2
WAITING TIME JITTER GENERATION IN DIGITAL MULTIPLEXERS

In this chapter, waiting time jitter generation in digital multiplex systems is discussed. The operating principles of time division multiplexing (TDM) and pulse stuffing synchronization are described. The definition and characteristics of waiting time jitter are presented. The accumulation of waiting time jitter in a chain of digital pulse stuffing multiplexers is briefly reviewed.

2.1 Time Division Multiplexing (TDM)

Time division multiplexing (TDM) is a process which interleaves several lower rate digital signals into a composite higher rate signal, to make efficient use of a wide band channel [1]. At the receiving terminal, demultiplexing performs the inverse operation, separating the higher speed pulse stream into lower bit rate signals, thereby recovering the original ones. A simple example of time division multiplexing is shown in Figure 2.1 [3]. The lower rate signals A and B are combined into a single higher rate signal C in the time division multiplexer. If the two signals have precisely the same bit rate (as shown in Figure 2.1b), their relative phase is constant, and the composite signal C is as shown in Figure 2.1c. However, if the input signal rates are not identical, the relative phase between the two signals is time varying. Inevitably, the two sets of input signal bits will, at times, overlap in the composite higher rate signal, as

shown in Figure 2.1d; as a result of the interference between the two data streams, signal information will be lost.

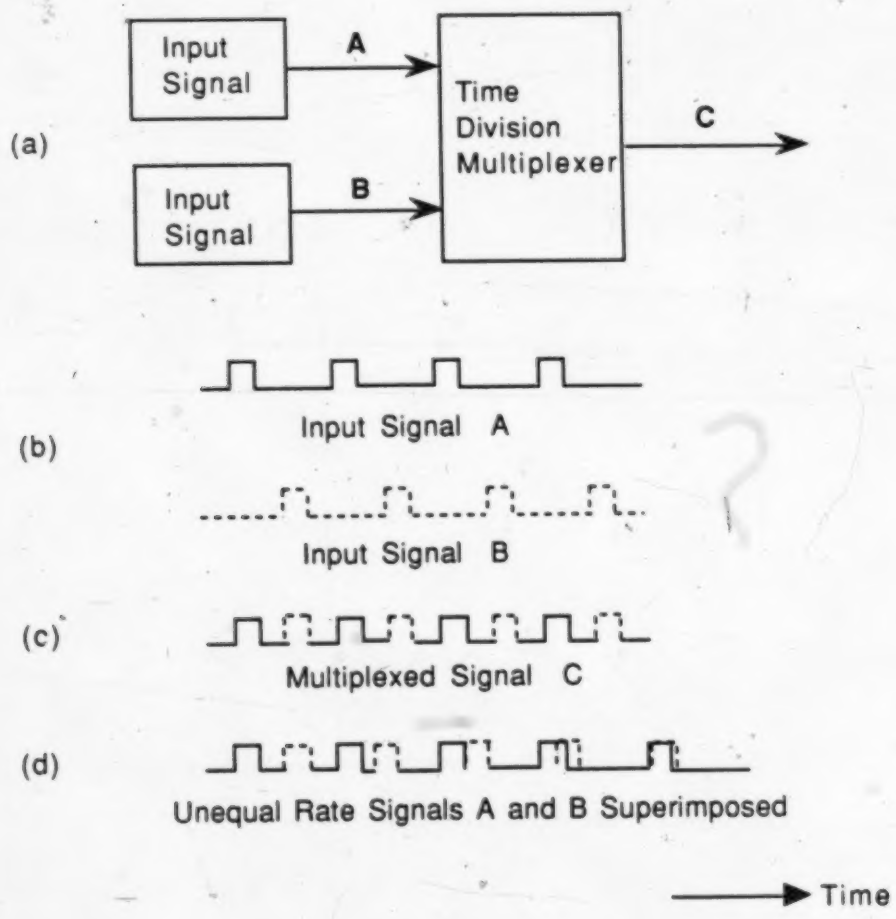


Figure 2.1 Example of time division multiplexing.

Because the sources of the various lower rate digital signals are often separated by large distances, these incoming signals normally do not use a common timing or clock signal. Rather, the incoming signals have the same *nominal* bit rate, but their *actual* bit rates vary within

certain prescribed tolerance limits. Such signals are referred to as *"plesiochronous signals"*. Before performing TDM, it is necessary to synchronize these plesiochronous signals, so that they can be properly interleaved and framed at the multiplexing terminal, and be properly identified at the demultiplexing terminal. There are several methods which can be used to realize this complex operation. In today's digital telephone networks, the most commonly used method is *pulse stuffing (or bit justification) synchronization* [4].

2.2 Pulse Stuffing Synchronization

In the pulse stuffing method of synchronization, the outgoing data rate of the multiplexer, controlled by the transmission system, is chosen to be slightly higher than the sum of the maximum rates of the incoming signals. This means that, for each lower rate signal, there are more data slots available at the higher rate than are actually required by the data. The extra capacity is used for overhead information and a small number of additional "dummy" bits. When these extra bits are added to each lower rate signal, their data rates are equalized, and they may be combined using TDM to produce the outgoing higher rate signal. Because the data rates have been equalized, there will be no overlap of data pulses (and consequent loss of data). The number of dummy or stuff bits added to each lower rate signal depends on their actual bit rate. Slower data rates require more dummy bit insertions. The concept of pulse stuffing synchronization is illustrated in Figure 2.2. The stuffed or dummy pulses are inserted at fixed time slot locations, called *stuff opportunities,* in a multiplex

frame format, so that they can be identified and removed at the demultiplexer. Overhead bits are introduced into the multiplex frame format so that the incoming signals can be easily demultiplexed. Since all incoming signals are pulse stuffed into identical-rate synchronous signals, time division multiplexing or switching can be performed.

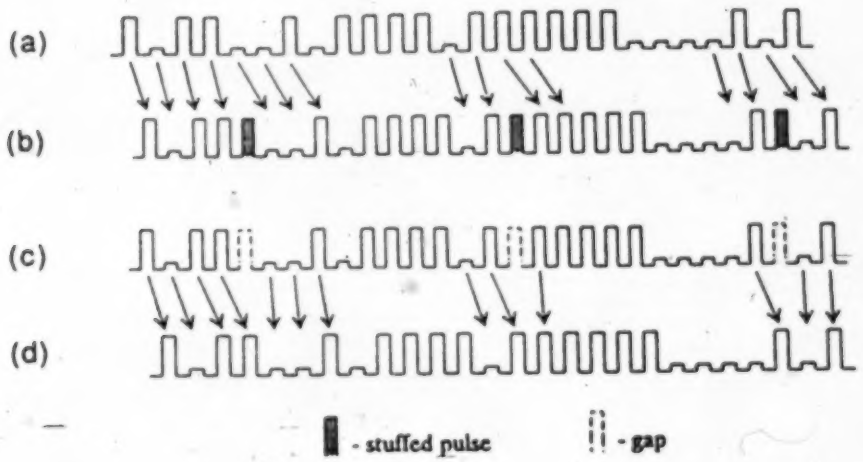


Figure 2.2 Example of pulse stuffing synchronization. (a) original signal, (b) stuffed signal to be multiplexed, (c) received and demultiplexed gapped signal, (d) recovered signal after PLL smoothing.

Pulse stuffing synchronization is a standard technique in the existing DS-X North American Digital Signal Hierarchy [5]. The following sample format is for a DS-1 (1.544 Mb/s) to DS-2 (6.312Mb/s) multiplexer (M12), which multiplexes four plesiochronous DS-1 digital signals into a DS-2 bit stream using pulse stuffing [1]. Referring to Figure 2.3, which shows one complete frame, the frame format consists

M_0 [48D] C_1 [48D] F_0 [48D] C_1 [48D] C_1 [48D] F_1 [$S_1D_2D_3D_4D_1D_2D_3D_4$.....D_3D_4]

M_1 [48D] C_2 [48D] F_0 [48D] C_2 [48D] C_2 [48D] F_1 [$D_1S_2D_3D_4D_1D_2D_3D_4$.....D_3D_4]

M_1 [48D] C_3 [48D] F_0 [48D] C_3 [48D] C_3 [48D] F_1 [$D_1D_2S_3D_4D_1D_2D_3D_4$.....D_3D_4]

M_1 [48D] C_4 [48D] F_0 [48D] C_4 [48D] C_4 [48D] F_1 [$D_1D_2D_3S_4D_1D_2D_3D_4$.....D_3D_4]

|←——— 48 bits ———→|

48D - 12 interleaved data bits from 4 DS-1 signals

S_n - stuff opportunity location for n'th DS-1 stream

C_n - stuff control bit for n'th DS-1

M_n - frame control bit

F_n - frame control bit

Figure 2.3 DS-1 to DS-2 (M12) multiplexing frame format.

of a periodic pattern, repeated twenty-four times, of a single overhead bit (an M, C, or F bit) followed by a sequence of twelve sets of four bit-interleaved, rate-equalized, DS-1 input signals. Thus the frame length is [24×(1+4×12)] = 1176 DS-2 bits. The M and F overhead bits are used for framing, and the C bits are control bits used to indicate the presence of stuff bits. Note that the stuff opportunities occur at the first data slot after the F1 bit. Figure 2.3 indicates these locations for the 4 DS-1 streams. If a stuff occurs, the bit position marked "S" is a dummy bit; when there is no stuff request, a data bit is sent in the normal way. At most, one stuff bit per channel can be inserted in each frame of 1176 bits. The maximum stuffing rate is, therefore, given by $\frac{6.312\ \text{Mb/s}}{1176} \cong 5.367$ kb/s.

Figures 2.4 and 2.5 illustrate the functional block diagrams for a typical multiplex synchronizer and desynchronizer, respectively [6].

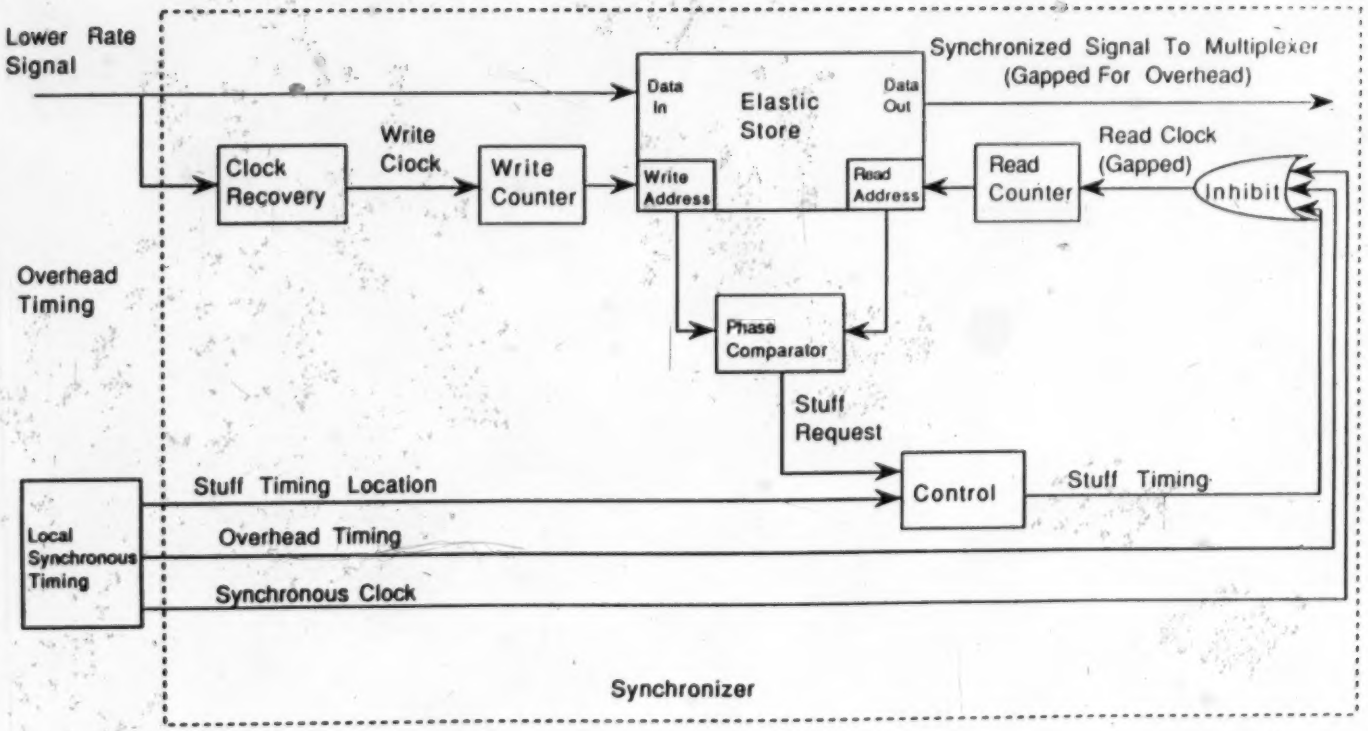


Figure 2.4 Block diagram of pulse stuffing synchronizer.

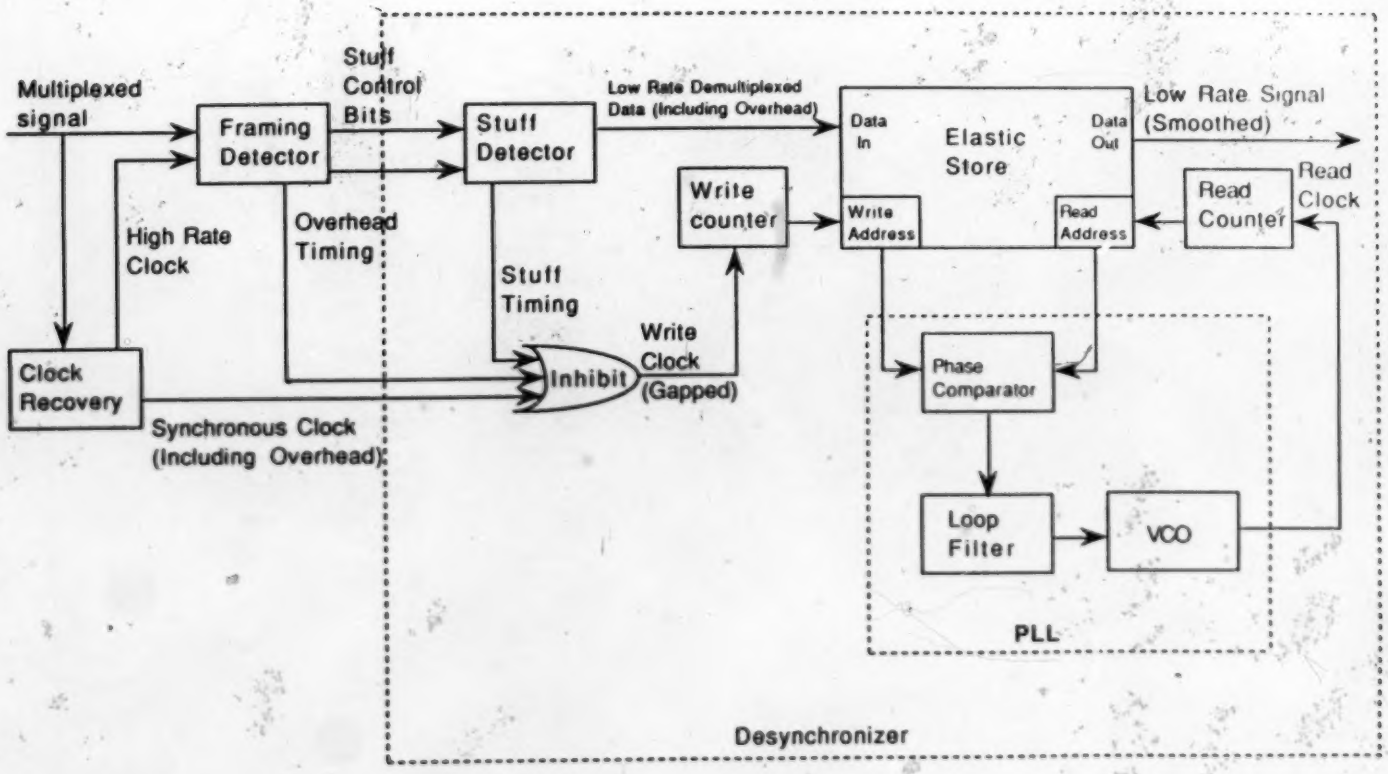


Figure 2.5 Block diagram of pulse stuffing desynchronizer.

At the synchronizer input, incoming tributary data are written into an elastic store [1] by an extracted clock and are read out of the store by a read clock at the synchronized output rate. The synchronizer phase detector (typically a D flip-flop) monitors the phase difference between the read and write clocks. When this phase difference reaches a predetermined threshold, the read clock is inhibited at the next stuff opportunity. Thus, a dummy data bit or stuff bit is inserted into the synchronized data output.

When the multiplexed signal is received, the dummy pulses are removed and each of the signals is retimed to smooth out the gaps. This is done by a desynchronizer for each signal stream. At the desynchronizer, a clock signal is derived from the demultiplexed data stream. Then the overhead timing and the stuff timing are inhibited, thus producing a clock gapped at the bit positions corresponding to the overhead and stuff bits. When the information signal is written into an elastic store by this gapped clock, only the data bits enter the store, and are available to be read out. Since we would like to read out the data at a uniform rate, the gapped clock must be "smoothed out". This is done using a phase-locked loop (PLL) circuit (whose characteristics will be discussed in Chapter 3). The PLL forces a voltage controlled oscillator (VCO) to adjust its frequency to the average rate of the incoming data, so that the original signal can be recovered. However, the PLL clock smoothing technique is imperfect, because phase-smoothing circuits have a low-pass nature. A low frequency timing noise impairment, called *waiting time jitter* [7] is present on the outgoing (lower rate) signals.

For multiplexing of plesiochronous signals, pulse stuffing is the least complex synchronization method, requiring the least amount of buffer storage. Because a possible deficit of up to only one pulse can be incurred before it is corrected at the next available stuffing opportunity time-slot, then, theoretically, only one bit of storage is required by the elastic store. In practice, a store size of several bits is normally used, due to various other factors [1]. Pulse stuffing also has the advantage that it is performed independently for each tributary signal and for each multiplexer, which improves the overall system reliability.

2.3 Waiting Time Jitter

Waiting Time Jitter is a low frequency phase jitter introduced whenever asynchronous digital signals are synchronized for multiplexing by pulse stuffing. It contains arbitrarily low frequency components, and cannot be completely removed from the demultiplexed signals [7].

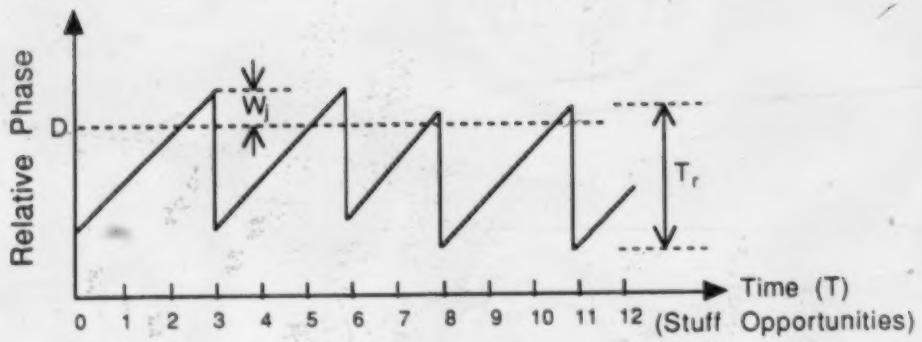
2.3.1 Defining Waiting Time Jitter

While pulse stuffing produces the obvious stuffing jitter (or justification jitter) of one time slot, a second, more subtle form of jitter occurs in pulse stuffed systems because stuffing can occur only at a fixed position in the multiplex frame format. Ideally, pulse stuffing should occur as soon as the stuff threshold is exceeded, but in fact the stuff bits are inserted at the fixed stuff opportunities so that they can be removed easily at the desynchronizer. This second

jitter component, due to the "waiting time" between stuff demand and stuff execution, constitutes waiting time jitter in the strict sense, but in practice no precise distinction between these two forms of jitter is made, and the term *"waiting time jitter"* is applied to both.

2.3.2 Waiting Time Jitter Generation

The basic cause of waiting time jitter, when pulse stuffing synchronization is used, can be explained as follows: At the synchronizer, the incoming lower speed data are written into the elastic store at frequency f_w and read out at the frequency of the local multiplexer clock f_r (f_r slightly greater than f_w). A phase comparator monitors the phase difference between the write and read clocks in order to make the stuff decision. The output of the phase comparator is the relative phase between these two clocks (or, equivalently, the jitter on the output data stream of the synchronizer). A typical waveform for the output of the phase comparator is shown in Figure 2.6. It is a simplified waveform because the effect of the overhead bits is not indicated. Due to the difference of the write and read clock frequencies, the phase error tends to increase linearly. When a stuff occurs, the phase error decreases by one read clock time slot, because the read clock is inhibited while the write clock continues. The phase error caused by the "waiting time", W_j, varies in an irregular quasi-random manner, and eventually contributes to the low frequency waiting time jitter components. A more exact waveform can be obtained by considering the effect of the overhead bits, which introduce some high frequency



T_r = one read clock time slot

D = threshold setting for pulse stuffing

Figure 2.6 Waiting time jitter waveform.

jitter components.

Assuming that the write and read clocks are regular, the slope of the relative phase waveform is a constant, which is determined by the two clock frequencies. For the M12 format, each signal has 12×6×4 or 288 positions per frame. The minimum number of data bits per frame is 277 (1 bit for stuffing), and the maximum is 288 (no stuffing). The actual data rate per frame is $288-\rho$, where ρ is the average number of stuffs per frame period. Since the maximum number of stuff pulses per frame is one, ρ is usually called the *stuff ratio*. The stuff ratio, ρ, is defined as the ratio of the actual number of stuff bits (average) to the maximum possible number of stuff bits. For example, in the M12 format, the nominal DS-1 rate f_1 is 1.544 Mb/s, and the standard DS-2 rate f_2 is 6.312 Mb/s. Because there are 12 DS-1 bits per channel out

of (1+12×4) = 49 DS-2 bits, the actual stuff rate is:

$$f_s = \frac{12}{49} f_2 - f_1 = \left(\frac{12}{49}\times 6.312 - 1.544\right)\times 10^6 = 1.796 \text{ kb/s}$$

The maximum possible stuff rate (i.e. the *stuff opportunity rate)* is:

$$f_m = \frac{f_2}{24\times 49} = \frac{6.312\times 10^6}{1176} = 5.367 \text{ kb/s}$$

Therefore, the nominal stuff ratio for the M12 format is:

$$\rho = \frac{f_s}{f_m} = \frac{1.796}{5.367} = 0.3346 \cong \frac{1}{3}$$

This means that one stuff occurs for, approximately, every three frames of data.

At the desynchronizer, a gapped clock is derived from the received signal, and a PLL circuit is used to remove the gaps and recover the original clock stream, as shown in Figure 2.5. The phase comparator (PC) of the PLL smoothing circuit monitors the phase difference between the gapped clock and the VCO output clock, and the phase difference is converted to a DC voltage applied to the control voltage terminal of the VCO. The VCO output frequency is, therefore, adjusted to reduce the phase or frequency difference between these two clocks. As discussed above, it is apparent that the jitter generated by stuffing (or justification) has much higher frequency components than that generated by the waiting time. Although the low-pass filtering action of the desynchronizer phase smoothing circuit usually eliminates the stuffing jitter, the frequency components of the waiting time jitter W_j are typically low enough to fall within the

phase smoothing circuit passband. Therefore, some of the low frequency phase jitter will remain on the recovered clock. Since any timing errors may cause bit errors at the final receiver, this clock jitter, present on the transmitted signal, may degrade the system performance (i.e. cause bit errors).

2.3.3 Waiting Time Jitter Characteristics

Waiting time jitter characteristics have been analyzed both in the time domain [8] and in the frequency domain [7]. In the time domain, the maximum amplitude of the waiting time jitter that may result for a given frame format, such as M12, can be estimated. Since the slope of Figure 2.6 is equal to ρ per frame, the amplitude of the waiting time jitter $W_{jmax} = \rho$. In the M12 format, there are 1176 DS-2 clock intervals between stuff opportunities. The maximum allowable DS-1 and DS-2 signal tolerances are ±130 ppm and ±33 ppm, respectively [6]. Therefore, the maximum difference frequency is obtained by using the maximum read clock frequency and the minimum write clock frequency. The maximum read clock frequency is:

$$f_{rmax} = 6.312000\times10^{6}\times(1 + 0.000033)\times\frac{12}{49} = 1.545847 \text{ Mb/s}$$

The minimum write clock frequency is:

$$f_{wmin} = 1.544000\times10^{6}\times(1 - 0.000130) = 1.543799 \text{ Mb/s}$$

The minimum time between stuff opportunities (or frame period) is:

$$t_s = \frac{1176}{6.312000\times10^6\times(1 + 0.000033)} = 186.3\ \mu s$$

Therefore, the maximum ρ per frame (i.e. maximum peak-to-peak value of the waiting time jitter) is:

(1.545847 - 1.543799) Mb/s × 186.3 μs = 0.38 bits.

The above jitter is relative to the synchronizer output. Depending on the jitter frequency components, this value will be reduced by desynchronizer filtering. Actually, $\rho \cong 1/3$ presents the worst case residual waiting time jitter after desynchronization, for the M12 format; the jitter amplitude is about 0.33 bits (at a very low frequency).

Waiting time jitter spectra have been derived by Duttweiler [7], and his experimentally recorded waiting time jitter spectra have supported that theory. The power spectral density of the waiting time jitter $\Phi_s(f)$, as a function of the stuff ratio ρ (considering the jitter as a stochastic process), is [7]:

$$\Phi_s(f) = \mathrm{Sinc}^2(f)Q(f) + \sum_{n=1}^{\infty}\left(\frac{\rho}{2\pi n}\right)^2\Big(\delta(f-n) + \delta(f+n)\Big) \qquad (2.1)$$

$$= \Phi_{s1}(f) + \Phi_{s2}(f)$$

where

$$\Phi_{s1}(f) = \mathrm{Sinc}^2(f)Q(f)\ , \qquad (2.2)$$

$$\Phi_{s2}(f) = \sum_{n=1}^{\infty}\left(\frac{\rho}{2\pi n}\right)^2\Big(\delta(f-n)+ \delta(f+n)\Big), \qquad (2.3)$$

$$\mathrm{Sinc}(f) = \frac{\mathrm{Sin}(\pi f)}{\pi f},$$

$$Q(f) = \sum_{n=1}^{\infty} \left(\frac{1}{2\pi n}\right)^2 \left[\mathrm{rep}\delta(f-\rho n) + \mathrm{rep}\delta(f+\rho n)\right], \qquad (2.4)$$

$$\mathrm{rep}X(f) = \sum_{k=-\infty}^{\infty} X(f-k), \quad \text{for any function } X(f).$$

and

$\delta(f)$ is the Dirac delta function,

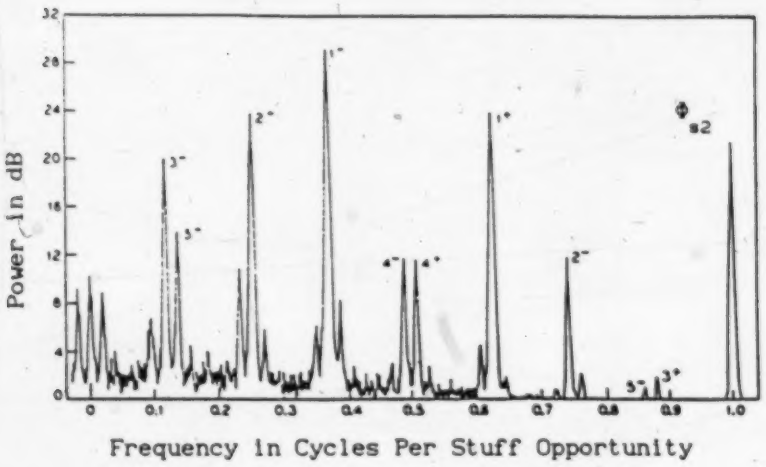
ρ is the multiplexer stuff ratio,

f is the jitter frequency normalized with respect to the stuff opportunity rate.

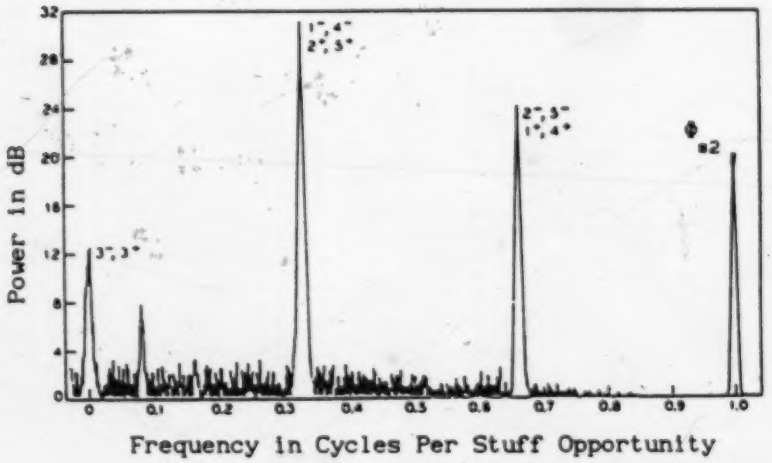
Eq. (2.1) shows that $\Phi_s(f)$ consists of two terms, $\Phi_{s1}(f)$ and $\Phi_{s2}(f)$. $\Phi_{s2}(f)$ contains only relatively high frequency components that can generally be easily filtered by the desynchronizer PLL circuit. The low frequency components of $\Phi_s(f)$ are contained in $Q(f)$. If ρ is irrational, none of the spectral lines overlap, as shown in Figure 2.7a [7]. However, if ρ is rational, for example, $\rho = \frac{p}{q}$ (p and q are small integers), the waiting time jitter pattern will repeat after some finite time. Then coincidence of the spectral lines occurs, as shown in Figure 2.7b [7]. For this case, $Q(f)$ can be expressed as a Fourier series giving a finite term sum [7]:

$$Q(f) = \frac{1}{4q^2} \sum_{n=1}^{q-1} \mathrm{Csc}^2\left(\frac{n}{q}\pi\right) \mathrm{rep}\delta\left(f - \frac{pn}{q}\right) + \frac{1}{12q^2}\,\mathrm{rep}\delta(f) \qquad (2.5)$$

Note that there are many distinct spectral lines in Figure 2.7. The n^- and n^+ notations on the figures correspond to the spectral lines introduced by the two terms of $Q(f)$, as given in Eq. (2.4).



(a) An experimental waiting time jitter spectrum with $\rho \cong 0.372$



(b) An experimental waiting time jitter spectrum with $\rho \cong 0.333$

Figure 2.7 Examples of experimental unfiltered waiting time jitter spectrum for a DS-1 to DS-2 multiplexer. (From Ref.[7])

If H(f) is assumed as the transfer function of the desynchronizer PLL circuit, the waiting time jitter on the recovered clock $\Phi_D(f)$ is:

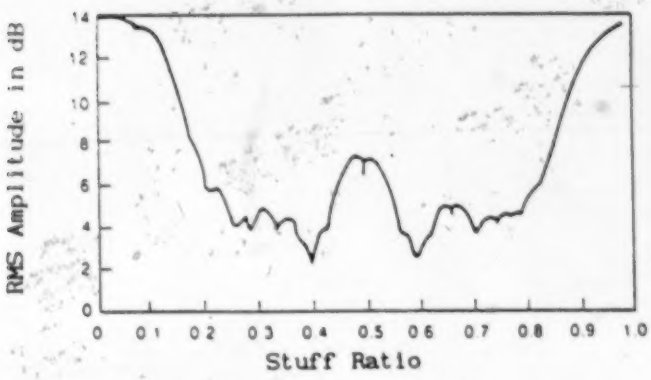
$$\Phi_D(f) = |H(f)|^2 \, \Phi_s(f) \tag{2.6}$$

with an rms amplitude σ_D of

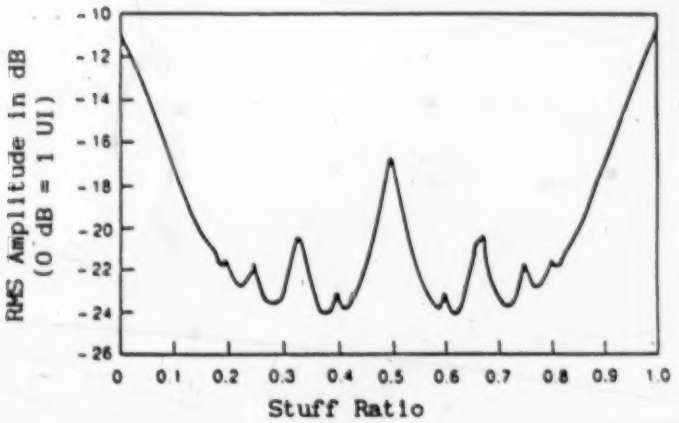
$$\sigma_D = \sqrt{\int_{-\infty}^{+\infty} \Phi_D(f) \, df} \tag{2.7}$$

Figures 2.8a and 2.8b reproduce the theoretical and experimental graphs for the rms waiting time jitter amplitude, as a function of stuff ratio for a DS-1 to DS-2 multiplexer [7]. The desynchronizer phase smoothing circuit used to obtain these results is a second-order filter with damping factor of 1.0, and a cut-off frequency of 644 Hz. The vertical (dB) scale does not correspond to any particular amount of jitter power, and is only relative. Note that the waiting time jitter power is strongly dependent on the choice of ρ. A stuff ratio near 0.0, 0.5, or 1.0 results in the generation of the largest (i.e. worst) amount of jitter. It should be emphasized that the jitter amplitude at these stuff ratios is due primarily to very low frequency components, that cannot be removed by the desynchronizer PLL circuit.

The results in [7] and [8] are based on the assumption that the overhead bits (F, M, and C bits) do not influence the stuff positions. In fact, a more accurate analysis shows that the overhead bits have an appreciable effect on waiting time jitter, increasing the number of frequency components in the jitter spectra, and enlarging the store size requirement [9]. The Fourier transform of the jitter waveform for



(a) An experimental graph of the rms amplitude of filtered waiting time jitter as a function of stuff ratio



(b) A theoretical graph of the rms amplitude of filtered waiting time jitter as a function of stuff ratio

Figure 2.8 Theoretical and experimental graphs of the rms amplitude of waiting time jitter as a function of stuff ratio ρ. (From Ref. [7])

this case has been derived for an M12 multiplex format [9], and a generalized pulse stuffing formula has also been derived by P.K.Chow [10]. Analyses in [11] give derivations of waiting time jitter characteristics, using various different methods, which agree in general with earlier published theory. Other work [12] has also shown that the presence of overhead bits in a multiplex format can cause measured jitter results to deviate significantly from the results obtained from the simple theory.

2.3.4 Waiting Time Jitter Accumulation

With the increasing digital interconnectivity of telecommunications networks, increasing attention is being given to the matter of jitter accumulation in long digital networks, both for network planning purposes and for equipment design. However, analysis of waiting time jitter accumulation is complicated because of the nonlinear interaction of the input jitter with the pulse stuffing process. Using random processes, Duttweiler has analyzed the effects of both sinusoidal and Gaussian input jitter on the jitter spectrum of the transmitted signal. These analyses provide a useful guide to what will happen in an actual long haul system. Analysis of the case of Gaussian input jitter is particularly relevant because the amplitude distribution of jitter for a long chain of digital repeaters is approximately Gaussian [13].

A question of much engineering interest concerns the manner in which waiting time jitter accumulates in a chain of multiplex-demultiplex pairs. An upper bound on the rms amplitude of

the waiting time jitter has been obtained by Duttweiler [7]. For a chain of N repeaters, he showed that the rms jitter will be no greater than $\sqrt{N/6}$ UI, provided that there is no peaking in any of the transfer functions of the desynchronizers in the chain. Thus, the accumulation rate of the waiting time jitter is not faster than the square root of N [7]. The measured characteristics of waiting time jitter have suggested that the probability density function (PDF) of jitter amplitude is a function of both the stuff ratio and of the input jitter characteristics [14]. Under the primary assumption that the jitter from each multiplexer can be modelled by a filtered Gaussian random variable, a frequency domain based model has been developed for predicting jitter accumulation in a series of cascaded multiplexers. The results from this model have been used to calculate the input jitter tolerance requirements necessary for equipment to successfully interface with the network [15].

Waiting time jitter generation and accumulation have been discussed in this chapter, and the significant problem that is presented is how to reduce this timing impairment in TDM systems. An approach [16] has been reported which employed a cancellation signal generator at the receiving terminal, driven by the stuff pulses [Figure 2.9]. The generator produces an output voltage which falls linearly, with a slope proportional to the average stuffing rate and having a positive step discontinuity each time a stuffed time slot appears. The output of the cancellation signal generator, which is the negative of the jitter component of the signal, is added to the phase comparator output of the elastic store, with the result that the

jitter associated with the received signal is, ideally, eliminated.

In Chapter 4, a new technique for reduction of waiting time jitter introduced by pulse stuffing will be investigated, and the experimental implementation will be described. Before that, Chapter 3 will briefly review some of the necessary theory required for the design of PLL clock recovery circuits.

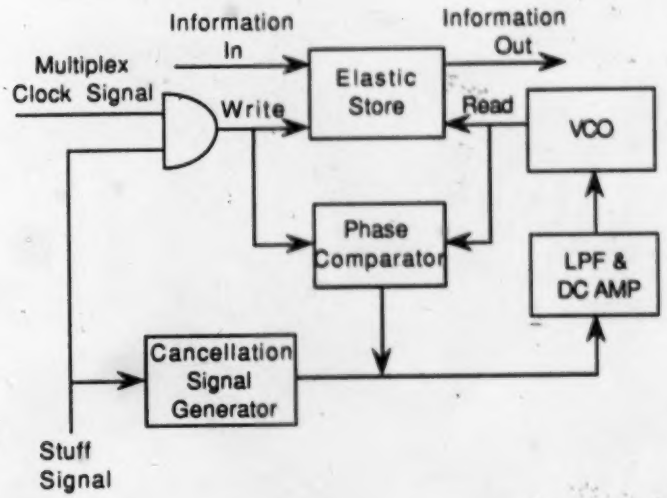


Figure 2.9 Block diagram of technique for reducing waiting time jitter in pulse multiplexing systems.

CHAPTER 3

PHASE-LOCKED LOOP THEORY

A phase-locked loop (PLL) contains three basic components as shown in Figure 3.1. These are:

(1) A phase detector (PD)

(2) A loop filter (LF)

(3) A voltage-controlled oscillator (VCO)

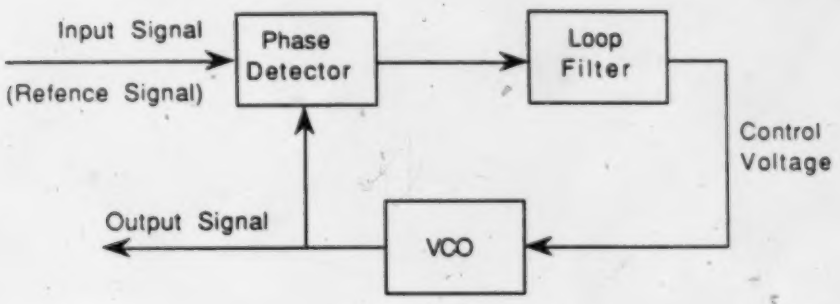


Figure 3.1 Basic phase-locked loop.

The phase detector compares the phase of an input signal against the phase of the VCO, and the output of the PD is a measure of the phase difference between its two inputs. The difference voltage is then filtered by the loop filter and applied to the VCO. The control voltage applied to the VCO changes the frequency in a direction that reduces the phase difference between the input signal and the VCO output.

A PLL circuit is frequently used to synchronize a locally

generated oscillator (the VCO) output signal with a reference or input signal, in frequency as well as in phase. When the loop is synchronized (called *locked*), the control voltage is such that the average frequency of the VCO is exactly equal to the average frequency of the input signal. In a well-designed loop, the steady state phase error between the oscillator's output and the reference signal is zero, or very small.

For a better understanding of the loop operation, we suppose that the incoming signal carries information in its phase and frequency. If this signal is noisy, the task of the PLL is to reproduce the original signal while removing as much of the noise as possible. This is a very useful property for clock recovery in digital data systems.

To reproduce the signal, the centre frequency of the VCO is set very close to the expected frequency of the signal. The waveforms of the VCO output and the incoming signal are compared by the phase detector, and the output of the phase detector is averaged over some length of time in order to suppress unwanted phase noise. This average voltage is used to establish the frequency of the oscillator. Therefore, if the input to the loop is a noisy signal, the output of the loop is a "clean" version of the input. The PLL is a kind of filter that passes signals and rejects noise.

Two important characteristics of the PLL are the frequency range over which the VCO can track or lock to the input signal, and the effective bandwidth (BW). These characteristics, discussed in this chapter, are also the key considerations for our experimental DPLL design described in the next chapter. The various PLL parameters such

as BW, loop gain, damping factor, and their effect on the transient behavior of the PLL will be discussed briefly. However, the detailed derivation of the equations for the various PLL parameters are not given, since the mathematical analysis is given in many textbooks [17, 18].

3.1 Operating Principles of the PLL

3.1.1 Basic Transfer Functions

Consider an elementary PLL, as shown in Figure 3.2. The input signal has a phase of $\theta_i(t)$, and the VCO output has a phase of $\theta_o(t)$. We assume that the loop is locked, that the detector is linear and that the PD output voltage is proportional to the difference in phase between its inputs; that is,

$$u_d = K_d(\theta_i - \theta_o) \tag{3.1}$$

where K_d is called the *phase detector gain factor* (V/rad).

The phase error voltage u_d is filtered by the loop filter, which has a transfer function F(s). The frequency of the VCO is determined by the control voltage u_f.

If a constant input voltage is applied to the VCO control input, the output frequency of the VCO remains constant. The deviation of the VCO from its centre frequency is $\Delta\omega = K_o u_f$, where K_o is termed the *VCO gain factor* (rad/s-V). The relationship between the VCO output frequency ω_o and control voltage u_f is:

$$\omega_o(t) = \omega_c + K_o u_f(t) \tag{3.2}$$

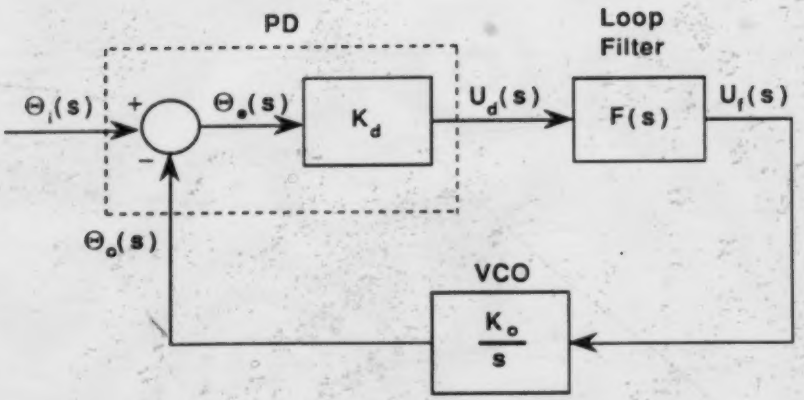


Figure 3.2 Block diagram of a PLL in the locked state.

where ω_c is the *nominal centre frequency* for $u_f = 0$. Since ω_c is a constant, then:

$$\frac{d\theta_o(t)}{dt} = K_o u_f(t) \tag{3.3a}$$

where θ_o is the output phase angle relative to ω_c. Therefore,

$$\theta_o(t) = \theta_o|_{t=o} + K_o\int_o^t u_f(t)dt \tag{3.3b}$$

In other words, the phase of the VCO output is linearly related to the integral of the control voltage. This inherent integration is represented by 1/s in Figure 3.2 (the term K_o/s).

The system, as depicted in Figure 3.2, is seen to be a classical linear feedback control system. Using the Laplace notation, the following equations may be derived [19]:

$$U_d(s) = K_d[\theta_i(s) - \theta_o(s)] \tag{3.4a}$$

$$U_f(s) = F(s)U_d(s) \tag{3.4b}$$

$$\theta_o(s) = \frac{K_o U_f(s)}{s} \tag{3.4c}$$

Combining these equations, the basic loop characteristics are obtained [19]:

$$\frac{\theta_o(s)}{\theta_i(s)} = H(s) = \frac{K_o K_d F(s)}{s + K_o K_d F(s)} , \tag{3.5}$$

where H(s) is the *closed-loop transfer function*. From Eq. (3.5), we obtain:

$$\frac{\theta_i(s) - \theta_o(s)}{\theta_i(s)} = \frac{\theta_e(s)}{\theta_i(s)} = 1 - H(s)$$

$$= \frac{s}{s + K_o K_d F(s)} \tag{3.6}$$

3.1.2 Second-Order Loop

Although there are various kinds of loops [20]; the most commonly used PLL is a second-order loop with a lag filter, because of its simplicity and good performance. The transfer function for the lag filter, as shown in Figure 3.3, is:

$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)} , \tag{3.7}$$

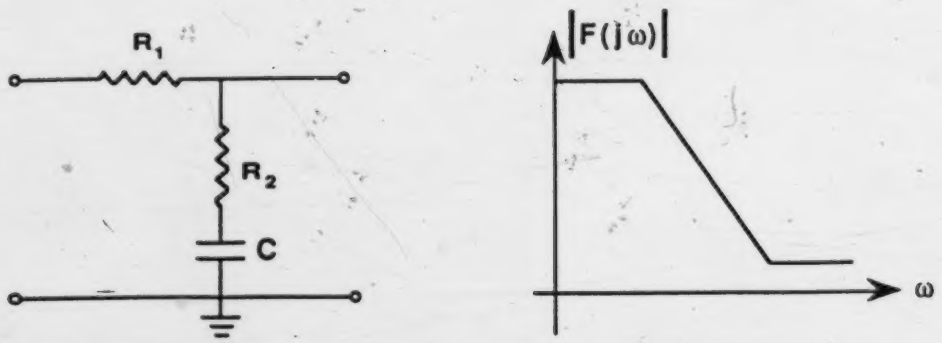


Figure 3.3 Lag filter and its transfer function.

where

$$\tau_1 = R_1 C \quad \text{and} \quad \tau_2 = R_2 C .$$

Substituting Eq. (3.7) into Eq. (3.5), we obtain:

$$H(s) = \frac{s\omega_n (2\xi - \omega_n / K_o K_d) + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} , \tag{3.8a}$$

where

$$\omega_n = \left(\frac{K_o K_d}{\tau_1 + \tau_2} \right)^{1/2} , \tag{3.8b}$$

and

$$\xi = \frac{1}{2} \left(\frac{K_o K_d}{\tau_1 + \tau_2} \right)^{1/2} \left(\tau_2 + \frac{1}{K_o K_d} \right) \tag{3.8c}$$

A second-order PLL is basically characterized by 3 main parameters, namely: the *natural frequency* ω_n, the *damping factor* ξ,

and the *loop gain* $K_o K_d$. If the optimized ξ is determined, ω_n and $K_o K_d$ can be chosen independently from Eqs. (3.8b) and (3.8c) by choosing the two time constants τ_1 and τ_2.

In Eq. (3.8a), if the loop gain $K_o K_d$ is much greater than ω_n, this PLL system is said to be a *high-gain loop*. Most practical PLLs are high-gain loops, in which case the transfer function of (3.8a) can be approximated as :

$$H(s) \cong \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{3.9}$$

The magnitude of the frequency response of a high-gain loop for several values of damping factor is plotted in Figure 3.4 [21]. It can be seen that the loop behaves as a low-pass filter. This means that the second-order PLL is able to track phase and frequency modulations of the reference signal as long as the modulation frequency is less than (about) ω_n. Therefore, the parameter ω_n is also called the *effective BW* of the PLL. There is an important frequency ω_{3dB} at which the jitter will be reduced by 3 dB. Its relation to the familiar concept of BW, ω_n, is presented in Eq. (3.10) [22].

$$\omega_{3dB} = \omega_n \left[2\xi^2 + 1 + \sqrt{(2\xi^2 + 1)^2 + 1} \right]^{1/2} \tag{3.10}$$

For example, for $\xi = 0.707$, $\omega_{3dB} \cong 2.06\ \omega_n$.

The damping factor ξ has an important influence on the dynamic performance of the PLL. For $\xi = 1$ the system is critically damped. If $\xi < 1$, the transient response becomes oscillatory. A low value of ξ

results in marked overshoot and relative instability of the loop. In many practical systems, the damping factor is chosen to be $\xi \cong 0.707$, which gives a slightly peaked frequency response.

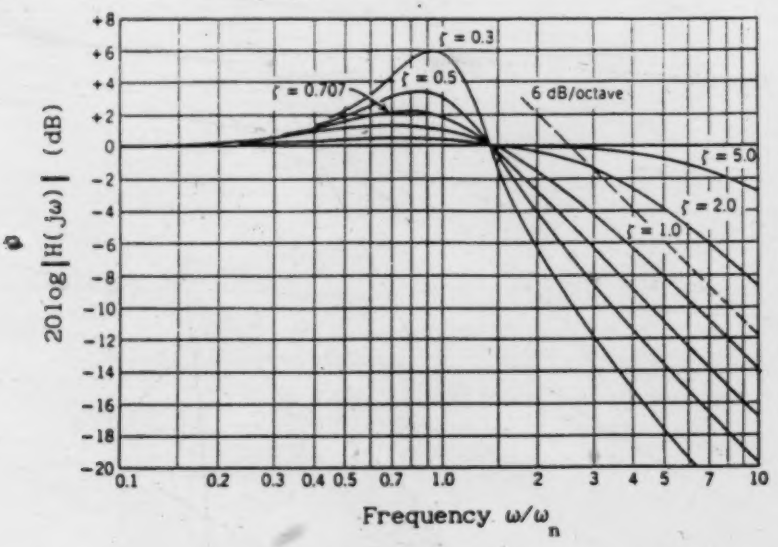


Figure 3.4 Frequency response of a high-gain second-order loop. (From Ref. [21])

3.2 PLL Components

There are basically two types of PLL commonly used, the linear or analog PLL and the digital PLL. In a linear PLL, both the reference and the output signals are sine-wave signals, which will have the same frequency when the PLL is locked. In a digital PLL, both the input signal and the output signal are binary digital signals, which have the same average pulse rates. In this type of PLL, analog functional blocks, such as RC loop filters and VCOs, are still used. The main difference between these two types of PLLs is that a different type of phase detector is used.

3.2.1 Phase Detector (PD)

There are four main types of phase detector that may be used in PLL circuits. These are:

Type 1: Linear phase detector (four-quadrant multiplier),

Type 2: The EX-OR gate,

Type 3: The edge-triggered JK flip-flop,

Type 4: The so-called phase/frequency detector.

Best has discussed how the various types of PDs affect the dynamic performance of PLL systems [23].

When the two inputs (or at least the reference signal) of the PLL are analog signals (i.e. sine-wave signals), a type-1 PD is usually used. Because this type of PD is insensitive to frequency error, it is primarily used for tracking phase information. Specifically, a PLL system utilizing this kind of PD is able to lock onto signals which are heavily buried in noise. The other three types of PDs are used in digital PLLs. The EX-OR gate, the simplest type, can only be used in applications where the waveforms are symmetrical, in which case the type-2 PD performs similarly to the type-1 PD except for the noise-suppression capability. The type-3 PD behaves very much like the type-1 PD when the reference signal frequency is approximately equal to the VCO output frequency. This type of PD is insensitive to the duty-cycle ratio of its input waveforms.

The type-4 PD is preferred in most digital PLL applications, because it is independent of the duty-cycle ratio of the input and output waveforms and, furthermore, when it is not phase locked, it will produce an output that is proportional to the frequency error,

$\Delta\omega$. This circuit as shown in Figure 3.5 is often referred to as a *phase/frequency detector*. As the frequency of the VCO will always be pulled in the correct direction, the pull-in range and the hold range of a PLL that makes use of such phase/frequency detector will, at least theoretically, be infinite [23]. Figure 3.6 illustrates the output waveform for this type of PD, and the output voltage as a function of phase error.

3.2.2 Loop Filter (LF)

Two widely-used loop filters for a second-order PLL are shown in Figure 3.7. The passive filter (Figure 3.7a has been discussed in Section 3.1.2) is quite simple and is often satisfactory for many applications. The active filter (Figure 3.7b) requires a high-gain DC amplifier, but provides better tracking performance.

The transfer function of the active filter shown in Figure 3.7b is:

$$F(s) = \frac{-A(sCR_2 + 1)}{sCR + 1 + (1 + A)(sCR)} \qquad (3.11)$$

For large A, this reduces to:

$$F(s) = -\frac{sCR_2 + 1}{sCR_1} = -\frac{s\tau_2 + 1}{s\tau_1}, \qquad (3.12)$$

where

$$\tau_1 = R_1C \quad , \quad \text{and} \quad \tau_2 = R_2C$$

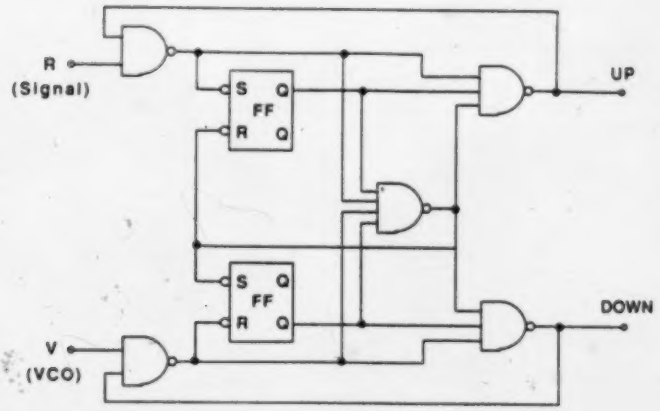
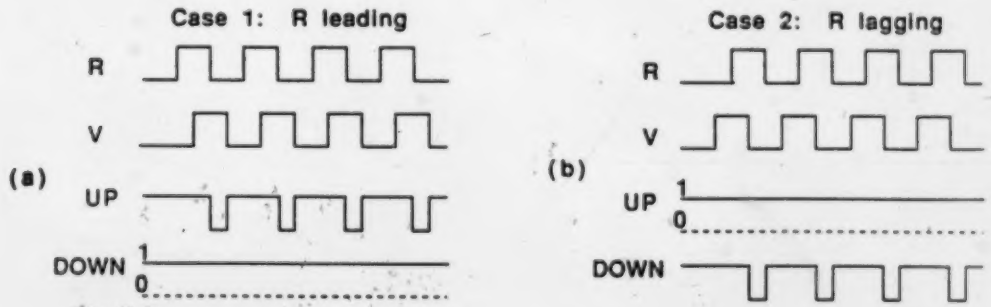


Figure 3.5 Schematic diagram of a phase/frequency detector.



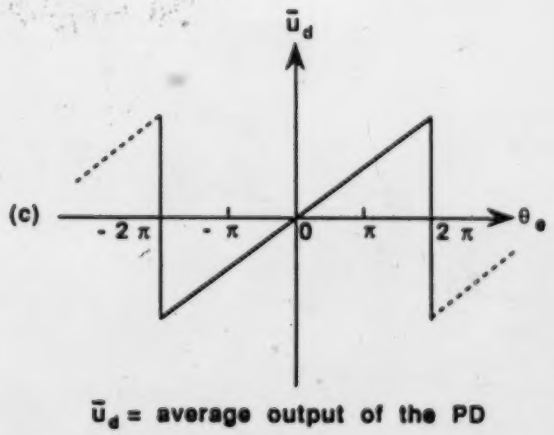
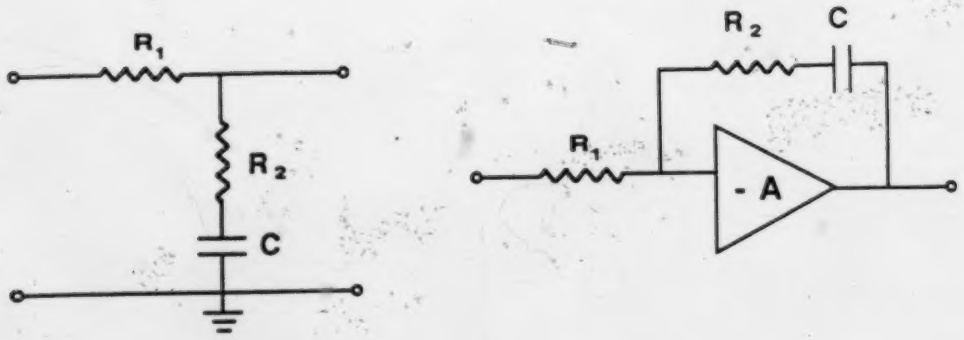


Figure 3.6 Output waveforms (a) and (b) and characteristics of a type-4 PD (c).



(a) Passive filter (b) Active filter

Figure 3.7 Filters used in second-order loops.

For the active filter, substituting Eq. (3.12) into Eq. (3.5), and allowing for the phase reversal of the amplifier, the closed-loop transfer function is found to be:

$$H(s) \cong - \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} , \qquad (3.13a)$$

where

$$\omega_n = \left(\frac{K_o K_d}{\tau_1} \right)^{1/2} , \qquad (3.13b)$$

and

$$\xi = \frac{\tau_2}{2} \left(\frac{K_o K_d}{\tau_1} \right)^{1/2} \qquad (3.13c)$$

Eq.(3.13a) is identical to Eq.(3.9). This indicates that a high-gain loop with a passive filter is, in fact, an approximation of a loop with an active filter.

Although better performance and better tracking can be achieved using active filters, precautions must be taken when employing them in a PLL circuit [24]. Undesired DC offset effects may drive the amplifier to its saturation limit, in which case self-acquisition (or frequency pull-in) cannot be easily achieved; the loop may never become locked, because a signal at the loop input may not be sufficient to bring the amplifier out of saturation. An aided acquisition technique, such as the frequency sweeping or the variable BW method, prevents saturation and helps the lock-in process [25]. Another more subtle difficulty can arise because the typical op-amp is not capable of handling high-frequency signals of large amplitude. Instead, it is affected by slew limiting. To avoid acquisition problems, the op-amp selected should minimize slew limiting.

3.2.3 Voltage-Controlled Oscillator (VCO)

There are many requirements placed on VCOs in different applications. Some of the more important requirements are as follows:

(1) Phase stability

(2) Large electrical tuning range

(3) Linearity of frequency versus control voltage

(4) Large gain factor (K_o)

(5) Low cost

There are four types of VCO in common use. These are:

(1) Crystal oscillators (VCXO)

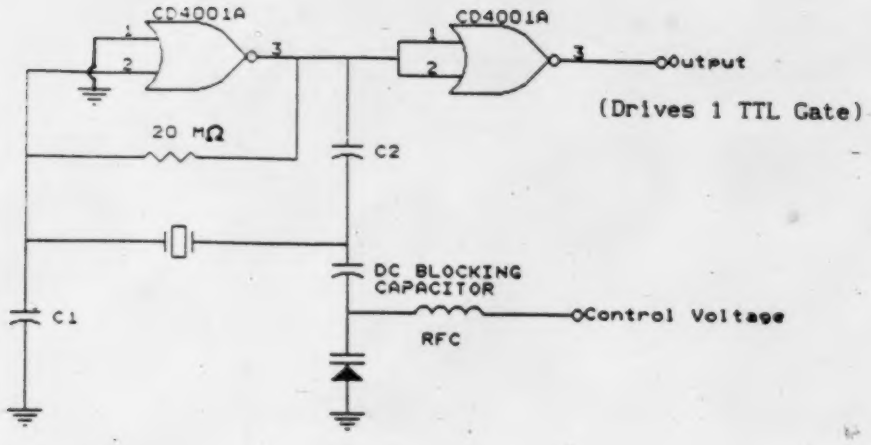
(2) Resonator (LC) oscillators

(3) RC multivibrators

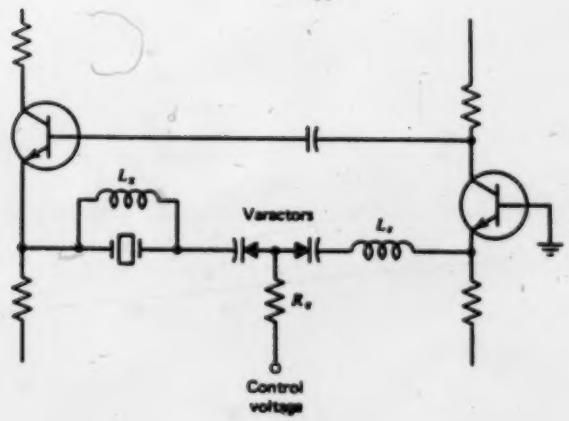
(4) YIG-tuned oscillators (at microwave frequencies)

When high-Q crystals are used in VCOs to achieve better phase or frequency stability, the tuning range of the oscillator is usually small, typically less than ±0.01% (or 100 ppm), depending on the type of crystal and the circuit used. To obtain a reasonable tuning range (greater than ±0.01% to ±0.02%) with good frequency stability, it is a common practice to use ordinary AT-cut crystals operating in their fundamental series-resonant mode. There are various circuits for VCXOs. The two circuits that we have tested in the lab are shown in Figures 3.8a and 3.8b. The single-gate oscillator is very simple and is recommended for use with TTL circuitry[26]. In the emitter-coupled oscillator, the varactor is in series with the crystal and allows the the resonant frequency to be varied over a comparatively large range [27]. The response time of the oscillation frequency to a changing control voltage depends only on how quickly the capacitance of the varactor can be changed.

If a wider tuning range (greater than ±0.25%) is needed, an LC oscillator must be used. Standard Hartley, Colpitts, and Clapp circuits, with varactor tuning can be used. The frequency stability for this type of VCO is not as good as for a crystal controlled oscillator, but a tuning range of a few percent can easily be obtained. Because of the poorer stability, this type of VCO may not be suitable for phase lock applications, although placing the VCO in an



(a) Single-gate oscillator



(b) Emitter-coupled oscillator

Figure 3.8 VCXO circuits

oven will provide some stability improvement.

When stability is of little importance, and a large tuning range is needed (up to ±33%), relaxation oscillators such as multivibrators are used. Multivibrators are available at very low cost as packaged integrated circuits. A high-frequency multivibrator has less time jitter than a low-frequency unit employing the same circuit topology (the timing capacitor is changed to set the frequency). Therefore, to reduce phase jitter, it is wise to operate a multivibrator at a frequency Nf_o, where f_o is the desired output frequency, and to then divide the output frequency by N. The phase jitter is then reduced by the factor N.

3.3 Tracking Performance of the PLL

To study the tracking performance of a PLL, the phase error $\theta_e(t)$ that results from a specified input $\theta_i(t)$ is examined. A small phase error is usually desired and is considered to be the criterion of good tracking performance.

3.3.1 Steady State Error

The phase error (in the frequency domain) is given by Eq. (3.6) as:

$$\theta_e(s) = \frac{s\theta_i(s)}{s + K_o K_d F(s)} \qquad (3.14)$$

The steady state error may be evaluated by means of the final value

theorem of the Laplace transform, which states:

$$\lim_{t\to\infty} y(t) = \lim_{s\to 0} sY(s) \tag{3.15a}$$

Therefore,

$$\lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} \frac{s^2\theta_i(s)}{s + K_o K_d F(s)} \tag{3.15b}$$

Consider the steady state error resulting from a step change of input phase of magnitude $\Delta\theta$. Then

$$\theta_i(s) = \frac{\Delta\theta}{s} \tag{3.16}$$

Substituting Eq. (3.16) into Eq. (3.15b)

$$\lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} \frac{s\Delta\theta}{s + K_o K_d F(s)} = 0 \tag{3.17}$$

In other words, the loop will eventually track any change of input phase; there is no steady state or long term error resulting from a step change of phase.

Next, let us examine the steady state error resulting from a step change of frequency of magnitude $\Delta\omega$. For this case, the input phase is a ramp $\theta_i(t) = \Delta\omega t$, so that

$$\theta_i(s) = \frac{\Delta\omega}{s^2} \tag{3.18}$$

Substituting Eq. (3.18) into Eq. (3.15b) results in:

$$\theta_v = \lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} \frac{\Delta\omega}{s + K_o K_d F(s)} = \frac{\Delta\omega}{K_o K_d F(0)} \qquad (3.19)$$

The product $K_o K_d F(0)$ is often called the *DC loop gain*, and is denoted by the symbol K_v.

Eq. (3.19) is useful when considering clock recovery, because the incoming signal frequency will never be exactly equal to the free-running (or centre) frequency of the VCO. As a result, there is a frequency difference $\Delta\omega$ between these two signals. Hence, the resulting phase error is given by $\theta_v = \Delta\omega/K_v$. If a high DC gain loop is used, a zero (or very small) static error for a step frequency change of the input can be achieved.

3.3.2 Transient Response

Besides steady state error, which is usually not a very important factor in clock recovery, it is often necessary to determine the transient behavior of the PLL for a particular input. It may be shown that if the parameters of the PLL are not well chosen, some ringing will occur during the transient response. A ringing transient response of a PLL used in a clock recovery circuit will cause timing jitter, which is undesirable. The dynamic responses of a second-order PLL to phase and frequency modulated reference signals have been analyzed and plotted by Gardner [28]. Figure 3.9 illustrates the transient phase error $\theta_e(t)$ due to a phase step $\Delta\theta$, and Figure 3.10 represents the transient phase error $\theta_e(t)$ due to a frequency step $\Delta\omega$. These responses are exact only for a high-gain loop.

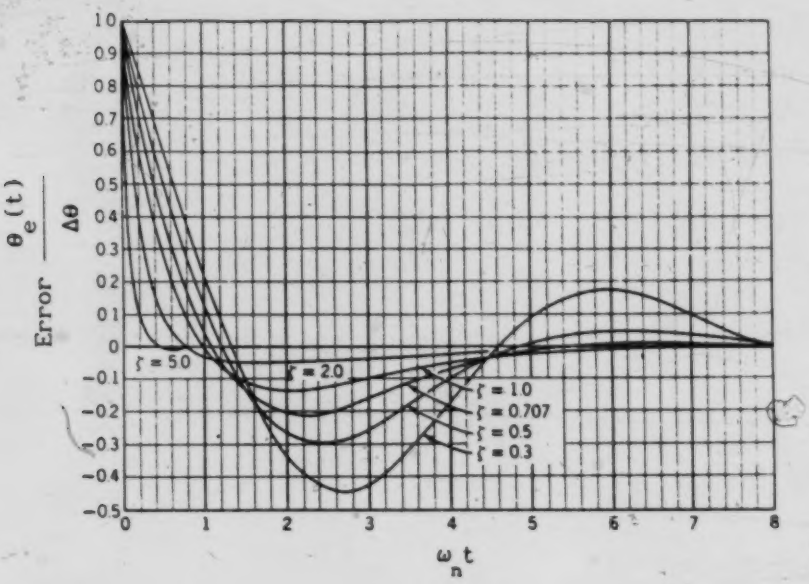


Figure 3.9 Phase error $\theta_e(t)$ due to a step in phase $\Delta\theta$. (From Ref. [28])

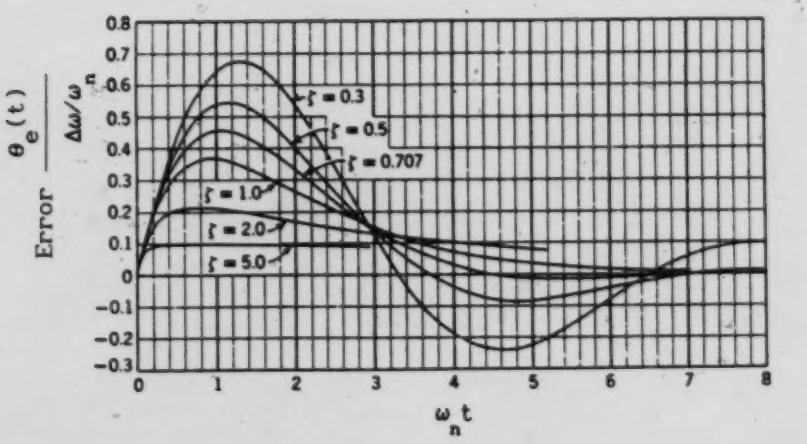


Figure 3.10 Transient phase error $\theta_e(t)$ due to a step in frequency $\Delta\omega$. (From Ref. [28])

Summary

In this chapter, basic concepts and principles of PLLs have been discussed. In a high gain second-order PLL, the loop response and BW can be adjusted independently, which allows optimization of the PLL parameters. This type of loop, using a lag filter, will be discussed in more detail in the next chapter.

CHAPTER 4
WAITING TIME JITTER REDUCTION IN AN M12 SYSTEM USING AN IMPROVED DESYNCHRONIZER

The way in which waiting time jitter is generated in TDM systems has been discussed in Chapter 2.

In this chapter, a new technique (or method) for clock recovery, which can achieve a reduction of waiting time jitter, is proposed [29]. This technique is described, and has been implemented in an experimental M12 system. The key to the new approach is using a DPLL circuit, which operates at the low frequency stuffing rate, so that very tight control of the recovered clock frequency can be obtained. Section 4.1 introduces M12 systems. Section 4.2 proposes the new desynchronizer for waiting time jitter reduction. Section 4.3 describes an experimental system. Section 4.4 presents measurement results of some important parameters of the DPLL circuit.

4.1 M12 Multiplexing Systems

As discussed in Chapter 2, M12 is a typical pulse stuffing multiplexer, whose simplified block diagram is shown in Figure 4.1. Four DS-1 rate data streams at the nominal bit rate of 1.544 Mb/s can be combined into one DS-2 rate signal of 6.312 Mb/s using pulse stuffing. Since $\frac{6.312 \text{ Mb/s}}{4}$ = 1.578 Mb/s, there are approximately 34,000 bits/s (1.578 Mb/s - 1.544 Mb/s = 34 kb/s) available for overhead and stuff bits. Of these, nearly 32,200 bits/s are used for framing and control bits. The stuffing rate is, in fact, approximately

1,800 bits/s (34,000 bit/s - 32,200 bits/s = 1,800 bits/s). These stuffing pulses follow an irregular pattern, occurring, on average, at a rate of about one stuff bit for every three frames of data.

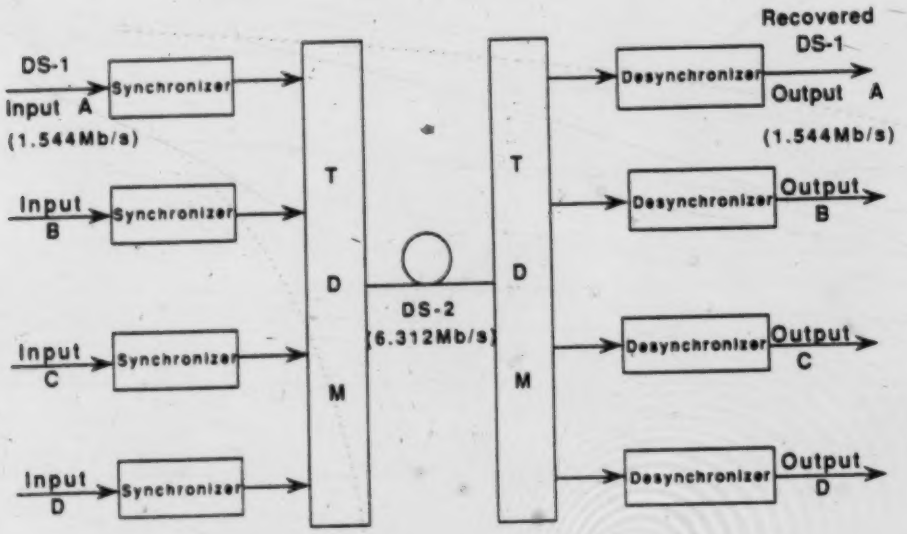


Figure 4.1 Block diagram of M12 multiplex systems.

At the demultiplexer terminal, the input frequency to the desynchronizer is 1.578 Mb/s. From this total number of bits, the overhead and stuff bits must be removed in order to recover the original data clock. In the desynchronizer, a gapped clock, therefore, must be produced in order that only the required data bits are read. Of these gaps, nearly 32,000 bits/s are due to the framing (M, F and C bits); these follow a regular pattern. The other approximately 1,800 bits/s are due to the pulse stuffing. These stuff gaps usually do not follow a regular pattern, because the nominal range of the stuff ratio is from 0.297 to 0.372. Depending on the stuff ratio, a stuff pulse

will occur approximately every three stuff opportunities, but with some occurring every two or four frames. Compared with the irregular stuffing pattern, the overhead gaps occur at a much higher frequency, and can be smoothed out easily by a PLL circuit.

Although existing M12 multiplex systems work at or near to the optimum stuff ratio (i.e. $\rho \cong \frac{1}{3}$), they suffer, however, from a certain amount of waiting time jitter impairment, which will vary depending on the design of the clock smoothing circuit.

In presently-used desynchronizers, the PLL clock recovery circuitry synchronizes with the gapped clock, and has as its output a reconstructed clock at, in principle, the actual input data rate. The stuffing pulse information is not directly used. For example, in M12 desynchronizers, the operating frequency of the PLL is about 1.544 Mb/s, with a loop BW of 350 Hz [15].

4.2 An Improved Desynchronizer with Reduced Waiting Time Jitter

A new approach, which utilizes an improved desynchronizer configuration, has been proposed for reducing the timing jitter present on the recovered data. The new desynchronizer circuit [Figure 4.2] makes use of the information (normally discarded) that is contained in the irregular stuff pulse stream. This new clock recovery circuit, named a *differential PLL* (DPLL), operates at the much lower bit rate of the stuff pulses, rather than at the higher bit rate of the gapped clock. For example, for an M12 format, the stuffing rate is approximately 1,800 bits/s, while the gapped clock rate is approximately 1.544 Mb/s. With the PLL operating at a much lower

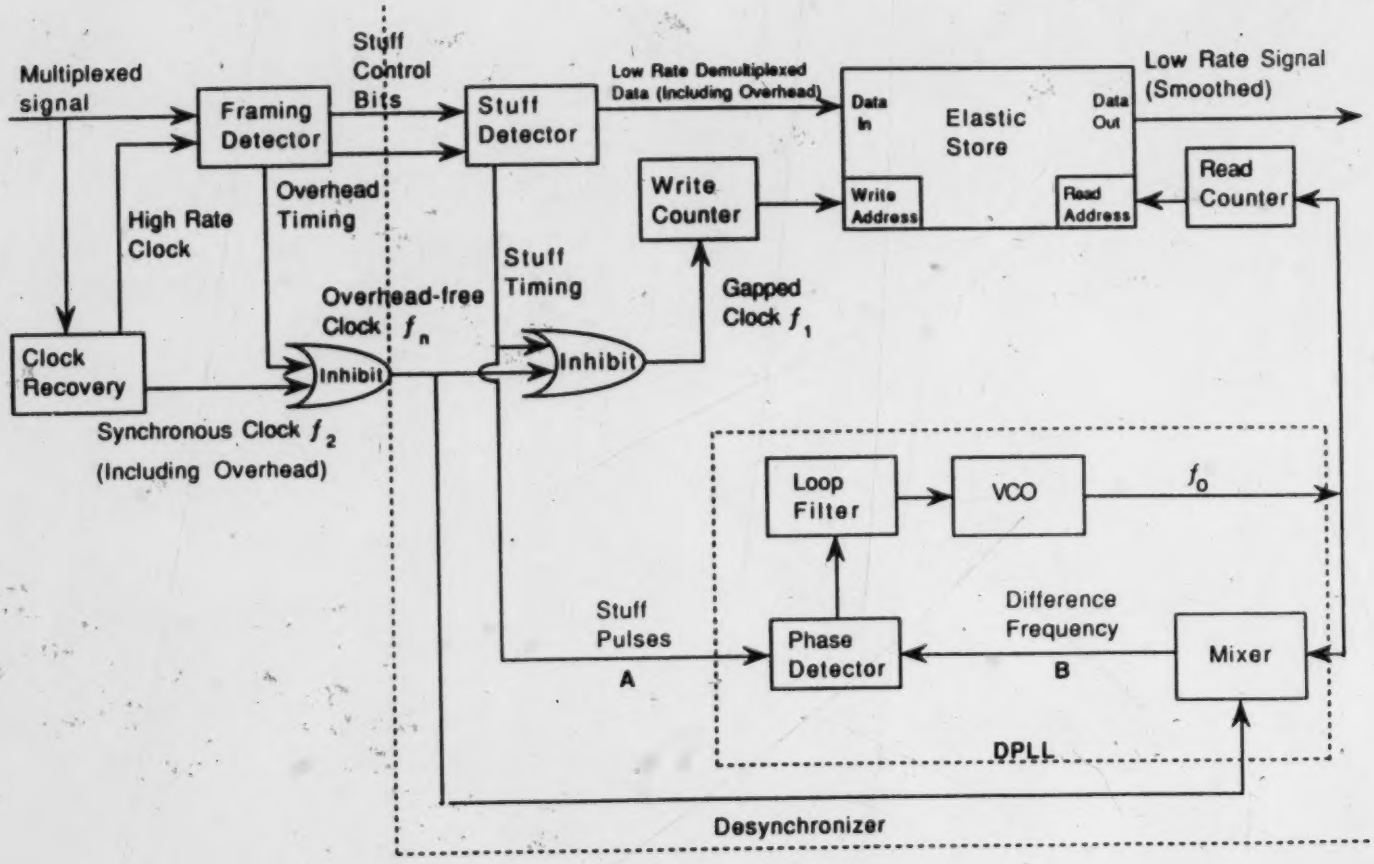


Figure 4.2 Improved desynchronizer for pulse stuffing multiplexing systems.

frequency, a very narrow bandwidth filter with high Q factor can be readily achieved, and thus very tight control of the VCO output frequency can be obtained. Therefore, the output clock jitter can be reduced, as compared to the presently-used clock recovery method.

The rationale behind the proposed circuit can also be perceived from frequency domain analysis. Consider two sample spectra of the waiting time jitter before PLL filtering for a DS-1 to DS-2 multiplexer, as shown in Figures 2.7a and 2.7b. These figures illustrate the unfiltered waiting time jitter spectra for a stuff ratio of 0.372, and 0.333, respectively. Because the vertical scale does not correspond to any particular amount of jitter power, we cannot predict exactly how much waiting time jitter can be filtered out by using a small bandwidth (BW) filter. But it is not difficult to anticipate that more waiting time jitter will be eliminated by narrowing the filter BW. The presently-used desynchronizers in M12 systems use a PLL BW of 350 Hz (0.065 cycles per stuff opportunity). In this project, we intend to design, construct and test a desynchronizer with a filter BW on the order of 10 Hz. We can expect that the residual waiting time jitter will, in general, be greatly reduced, since we know that the waiting time jitter frequency components are typically from 10 Hz to 1 kHz [30]. For certain critical stuff ratios (i.e. close to 1/3), the jitter power spectrum contains very low frequency components (extending to DC), which cannot be filtered out even if a very narrow BW filter is used.

There are several advantages for this new desynchronizer configuration:

(1) In present desynchronizers, the PLL operates at the data rate of the recovered clock (for M12 systems, 1.544 Mb/s). Compared with the gapped clock f_1 (or the output clock f_0), the stuff rate is much slower (typically 1,800 bits/s for the M12 format). Because low frequency signals are used to control the PLL clock recovery circuit, it is relatively easy to design a stable high-gain loop with a high Q-factor.

(2) Also, because of the low frequency, the PLL can synchronize easily with the incoming signal. For high operating frequencies, the pull-in process of a PLL with a narrow BW filter can be very slow (see Appendix I), or may not happen at all, as a result of undesired DC offsets.

4.3 Experimental Circuit Setup

We have not attempted to build a complete M12 experimental multiplexing system. In order to test the jitter performance of the proposed desynchronizer, an experimental system, basically consisting of a generator for the stuff pulses and a DPLL clock recovery circuit, has been built. The following subsections describe the circuitry in detail.

4.3.1 Generator for the Stuff Pulses and the Gapped Clock

From Figure 2.5, we can see that a desynchronizer basically consists of recovery circuitry for the gapped clock, a PLL clock recovery circuit, and an elastic store. In the improved desynchronizer of Figure 4.2, both the stuff pulses and the gapped clock are used for

recovering the original signal. The circuitry required to produce the stuff pulses and the gapped clock (both of these signals are available in the presently-used desynchronizer) for the new desynchronizer is shown in Figure 4.3.

Figure 4.3 illustrates the block diagram of the generator for the stuff pulses and the gapped clock. Using an HP 3325A Synthesizer/Function Generator and a Wavetek 178 Waveform Synthesizer, and assuming these to be jitter free, we produce a standard DS-1 rate clock and a standard DS-2 rate clock. The DS-2 clock is first inhibited for overhead bit occurrences, then divided by 4. An overhead-free clock f_n at the bit rate of approximately 1.5458 Mb/s is obtained. The stuff detector consists of a phase comparator MC4044 and a D flip-flop. When the phase difference of the gapped clock and the reference DS-1 clock reaches a predetermined threshold, the stuff "flag" is set. At the next stuff opportunity, which is at a fixed location in each frame, a stuff pulse is generated (see Figure 4.4a). The stuff pulses are then inhibited (gapped) from the overhead-free clock f_n, producing a gapped clock f_1 (see Figure 4.4b), whose average bit rate is equal to the original DS-1 signal bit rate; in the desynchronizer, it is this fully gapped clock that writes the data bits into the elastic store.

The circuit of the generator for the stuff pulses and the gapped clock is built on a printed circuit (PC) board. Standard TTL integrated circuit chips are used throughout. The circuit operation is very stable.

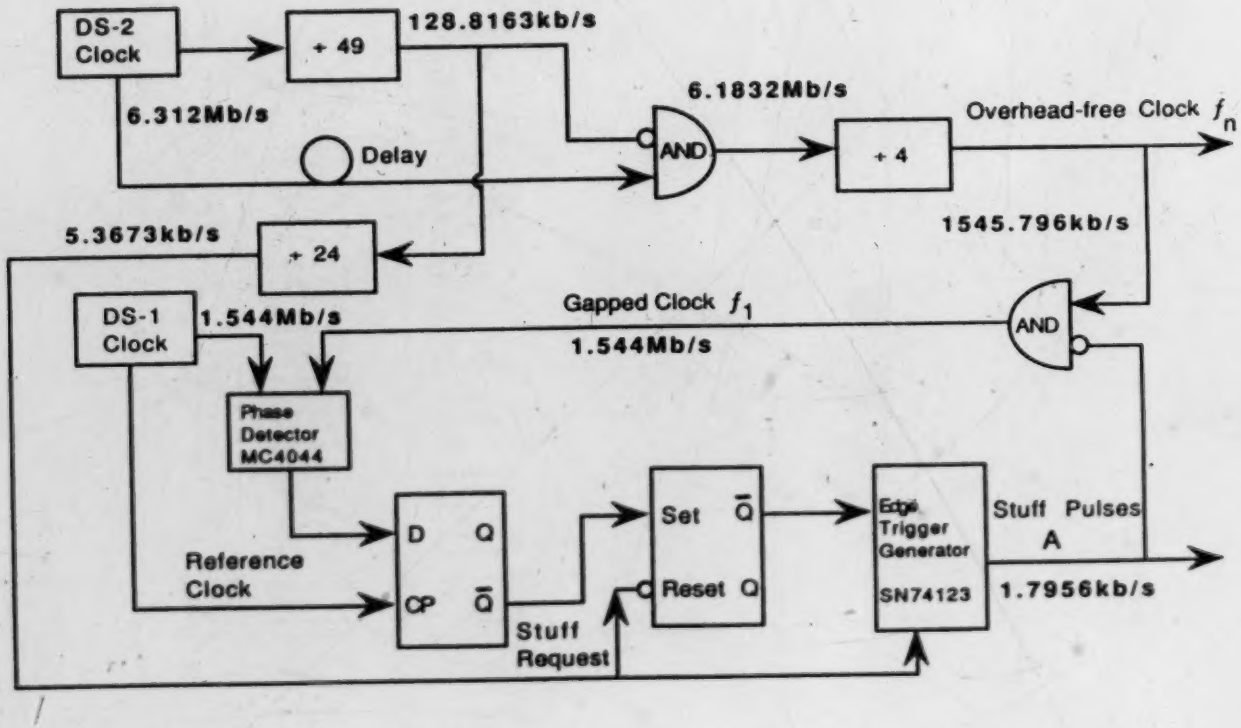
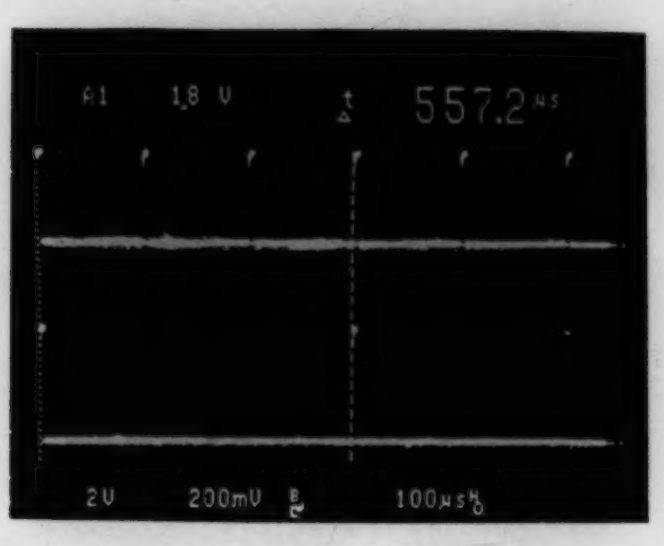
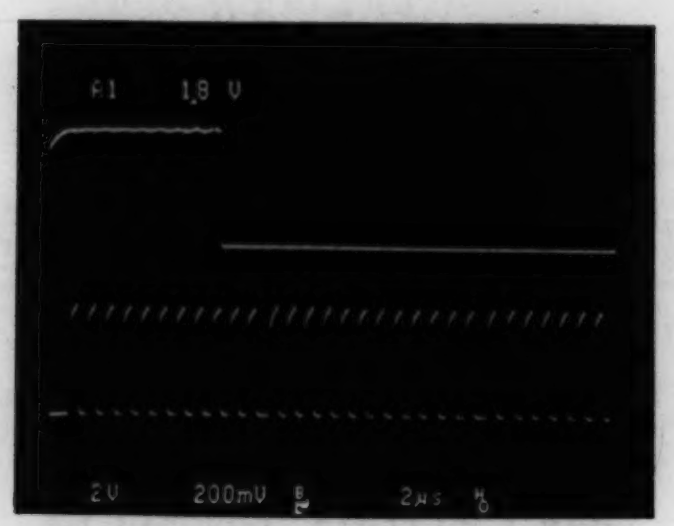


Figure 4.3 Generator for the stuff pulses and the gapped clock.



(a) The stuff opportunity signal (top trace) and the stuff pulse signal (lower trace), for DS-1 rate of 1.544000 MHz.



(b) The widened stuff pulse (top trace) and the gapped clock (lower trace).

Figure 4.4 The outputs of the generator for the stuff pulses, and of the gapped clock.

4.3.2 DPLL Clock Recovery Circuit

In our proposed new desynchronization method, a DPLL clock recovery circuit is employed, so that the low-frequency stuff pulse stream is used to control the PLL operation instead of the higher-rate gapped clock. The schematic diagram of the DPLL circuit is illustrated in Figure 4.5. Basically, this clock recovery circuit consists of a digital PLL and a mixer. The digital PLL consists of a phase/frequency detector, a loop filter, and a VCO. The centre frequency of the VCO is set at 1.544000 MHz. The loop filter's output voltage controls the frequency of the VCO, so that the average rate of the recovered clock is equal to the original DS-1 clock rate. The phase/frequency detector monitors the phase and frequency difference of the stuff pulses A and the difference frequency B, and converts the digital output to an analog voltage, which is added to the control voltage of the VCO. The digital mixer, consisting of an MC4044 and an RC low-pass filter, converts the higher rate of the recovered clock at the rate of 1.544 Mb/s, to the difference frequency at the rate of approximately 1,800 bits/s.

In order to obtain significant jitter suppression, the DPLL circuit needs to be carefully designed. The three parameters, ω_n, ξ and $K_o K_d$, must be selected properly so that good dynamic response can be achieved for a narrow BW filter with a high DC gain. The detailed design of the DPLL circuit is discussed in the following subsections. A mathematical model of the DPLL circuit is established first. Then the design of the circuit components, namely the phase detector, the VCO, and the loop filter are discussed, and the effects of the loop BW

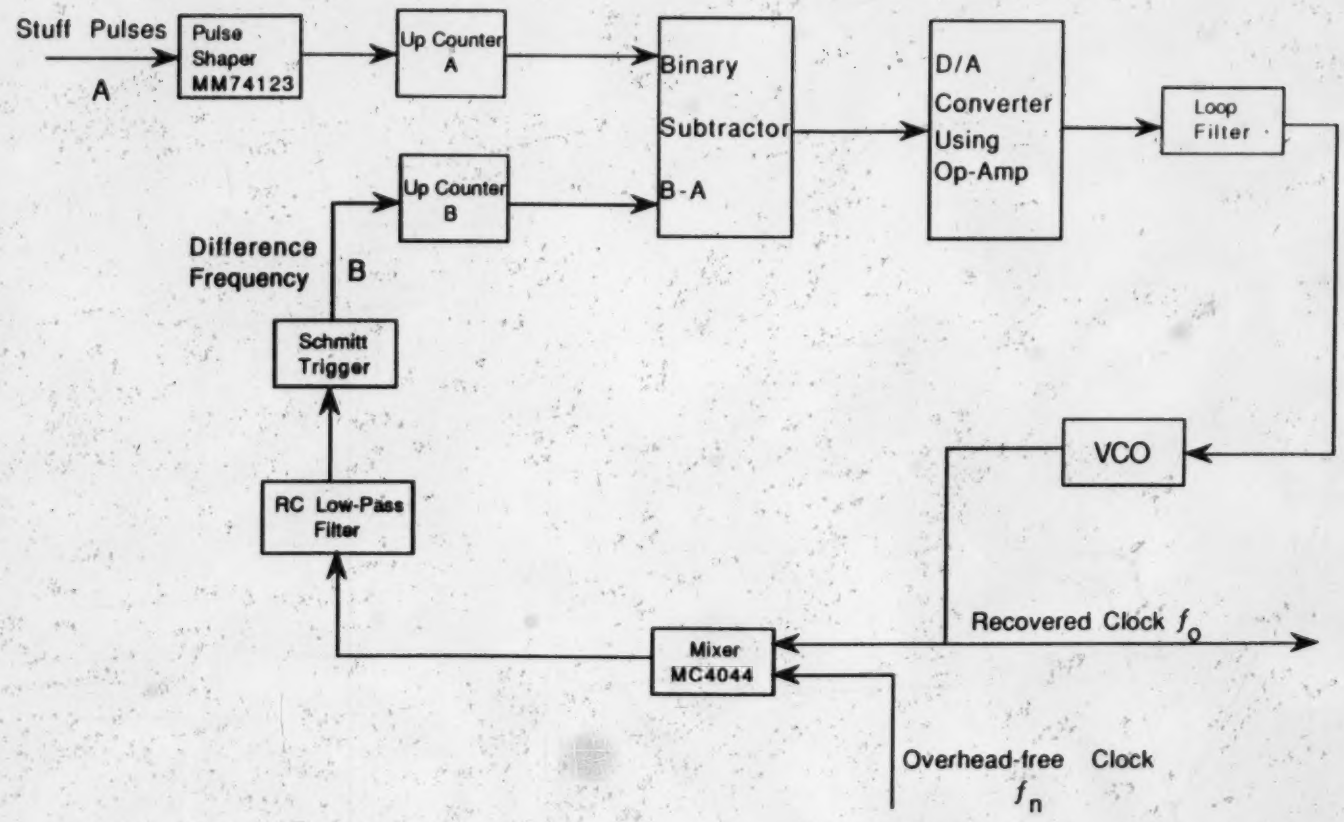


Figure 4.5 Schematic diagram of the DPLL clock recovery circuit.

on the PLL performance are determined.

4.3.2.1 Modelling the DPLL Circuit

A mathematical model of the DPLL circuit (or a linearized block diagram of the DPLL in the complex frequency domain) is shown in Figure 4.6.

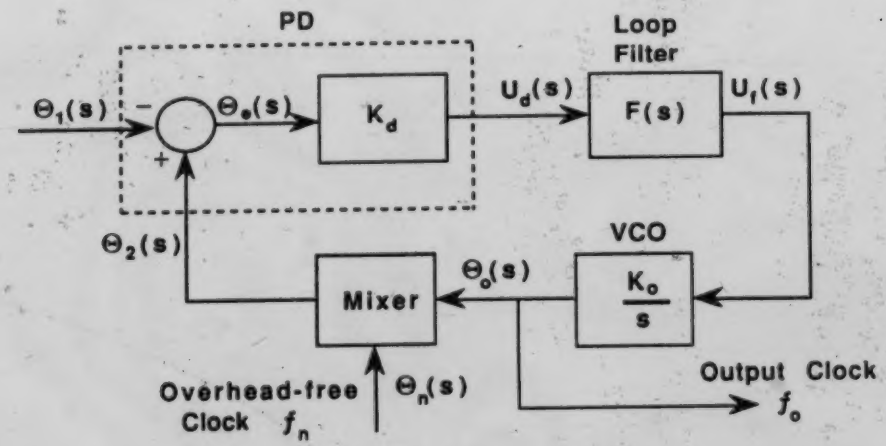


Figure 4.6 Block diagram of the DPLL circuit.

The transfer function for the various functional blocks are:

- Phase detector $$\frac{U_d(s)}{\Theta_e(s)} = K_d \qquad (4.1)$$

- Loop filter $$\frac{U_f(s)}{U_d(s)} = F(s) \qquad (4.2)$$

- VCO $$\frac{\theta_o(s)}{U_f(s)} = \frac{K_o}{s} \qquad (4.3)$$

- Mixer $$\theta_n(s) - \theta_o(s) = \theta_2(s) \qquad (4.4)$$

Because the overhead-free clock f_n is a constant clock signal, $\theta_n(s) = \Delta\omega_n t = 0$. Therefore, Eq. (4.4) becomes:

$$\theta_2(s) = -\theta_o(s) \qquad (4.5)$$

Combining these equations, the loop transfer function may be obtained:

$$H(s) = \frac{\theta_2(s)}{\theta_1(s)} = \frac{K_o K_d F(s)}{s + K_o K_d F(s)} \qquad (4.6)$$

This equation is identical to Eq. (3.5). Therefore, the characteristics of the DPLL circuit are identical to the PLL characteristics discussed in Chapter 3.

4.3.2.2 VCXO Design

To minimize the jitter on the recovered clock, the VCO itself should be inherently very regular and stable. Various circuits were tried in order to find one that would give satisfactory operation. For good short-term stability, a voltage-controlled crystal oscillator (VCXO) is preferred. The circuit shown in Figure 3.8a has been built and tested. A parallel-mode crystal with a nominal centre frequency of 1.544100 MHz has been used. The values of the capacitors C_1 and C_2 are 68 pF and 47 pF, respectively. A varactor (IN5450A) is used for

electronic tuning of the oscillator frequency. The circuit worked as expected (the output frequency changed with the variable control voltage), but the linearity of this circuit is not good, and the tuning range is not wide enough (from 1543.993 kHz to 1544.126 kHz, corresponding to the control voltage from 0 V to 16 V). The emitter-coupled oscillator of Figure 3.8b has also been investigated. A series-mode crystal with a nominal centre frequency of 1.544100 MHz has been used. This circuit is difficult to adjust. Sometimes L_x resonates with the varactors, in such a way that the crystal loses control of the oscillation frequency.

Because the tuning range of the VCXO is required to be at least ±200 Hz, centred at 1.544 MHz [6], this VCXO is implemented by means of a crystal controlled multivibrator MC4024; this gives both good frequency stability and a fairly reasonable tuning range. The nominal centre frequency of the crystal is 12.36 MHz (approximately $8f_{DS-1}$). The VCXO is thus built using a MC4024 followed by a divide-by-8 circuit, as shown in Figure 4.7.

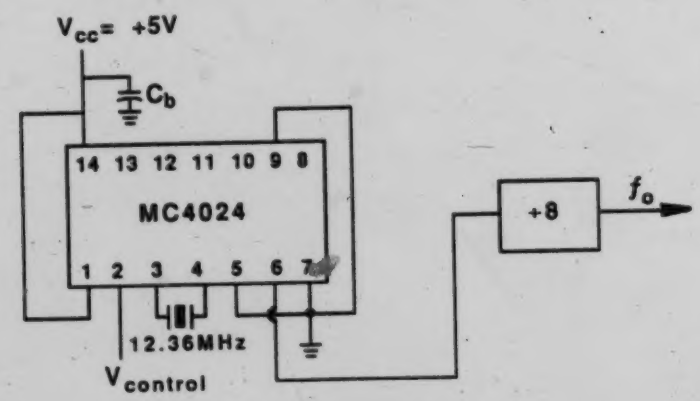


Figure 4.7 Circuit diagram of the experimental VCXO.

The frequency of this VCXO can be varied from 1543.784 kHz to 1544.210 kHz, for an input voltage range of 3.71 Volts to 3.89 Volts, resulting in a gain of $K_o \cong 15000$ rad/s-V. The centre frequency is 1.544 MHz for a control voltage of 3.80 Volts.

4.3.2.3 Phase Detector Design

A type-4 phase/frequency detector, such as the MC4044, can be used in the system. However, as shown in Figure 3.6c, the locked operating range of this PD is $\pm 2\pi$. In order to allow a greater range of operation (up to $\pm 4\pi$ phase difference), a simple phase detector has been implemented using two three-bit up-counters, a subtractor, and an operational amplifier circuit. The circuit diagram is shown in Figure 4.8. A reference voltage of -12 V is used to set a DC voltage offset of +4 V on the PD output, which is compatible with the control voltage of the VCO for the centre frequency. The state S_n = "1" corresponds to 3.5 V, and the state S_n = "0" corresponds to 0 V. The overall output voltage is, therefore,

$$u_d = 3.5\times\left(\frac{10}{35} S_2 + \frac{10}{70} S_1 - \frac{20}{35} S_3\right) + \frac{20}{60}\times 12$$

$$= 3.5\times\left(\frac{1}{7} S_1 + \frac{2}{7} S_2 - \frac{4}{7} S_3\right) + 4$$

$$= \frac{1}{2} (S_1 + 2S_2 - 4S_3) + 4$$

In general, the output u_d can take on eight voltage levels. They are:

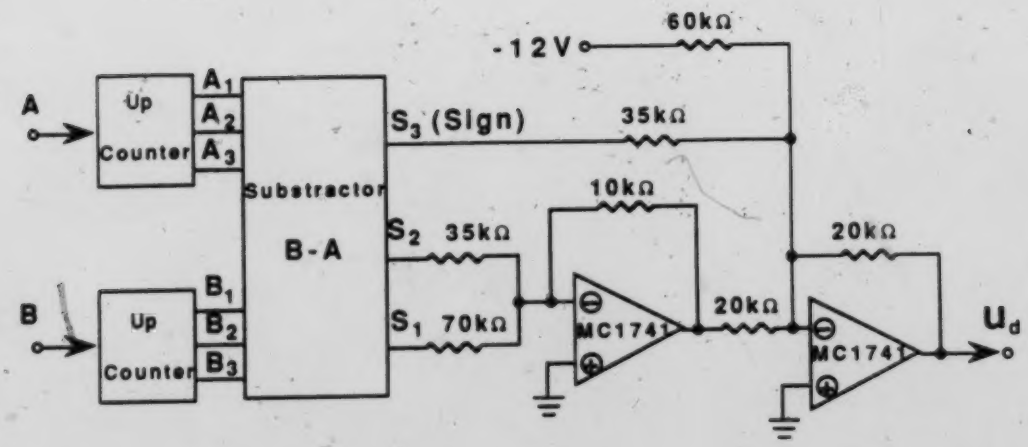


Figure 4.8 Circuit diagram of the experimental PD.

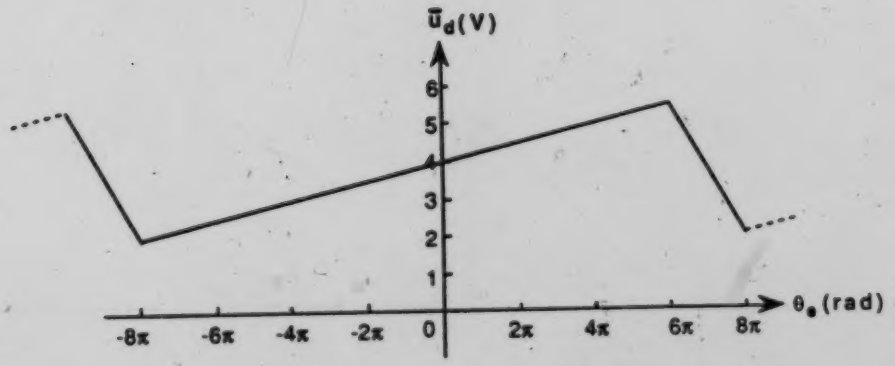


Figure 4.9 Average PD output $\bar{u}_d$ as a function of phase error θ_e.

State				Output Voltage
S_3	S_2	S_1	S	u_d(V)
1	0	0	-4	2.0
1	0	1	-3	2.5
1	1	0	-2	3.0
1	1	1	-1	3.5
0	0	0	0	4.0
0	0	1	+1	4.5
0	1	0	+2	5.0
0	1	1	+3	5.5

where

$$S = S_1 + 2S_2 - 4S_3$$

When the PLL is in the locked state, then only part of this table (i.e. output voltage range between +3 V to +5 V) is usually used.

The average output voltage $\bar{u}_d$ as a function of phase error θ_e is shown in Figure 4.9. Because the two inputs of this PD, the gapped pulses A and the difference frequency B, are supposed to have the same average bit rate in the locked state, there will probably be no more than a $\pm 2\pi$ phase difference (i.e. one pulse out). However, the greater operating range of $\pm 4\pi$ will help the lock-in process of the DPLL when the frequency of the reference signal to the DPLL is changed. By definition, the PD gain K_d is equal to the variation of the PD output voltage related to its phase error variation. For the experimental PD circuit, therefore:

$$K_d = \frac{\Delta \bar{u}_d}{\Delta \theta_e} = \frac{0.5}{2\pi} = 0.0796 \text{ V/rad} \cong 0.08 \text{ V/rad.}$$

4.3.2.4 Loop Filter Design

In order to test the basic principles of operation of the new circuit, a lag filter (Figure 3.3) with the transfer function of Eq. (3.7) has been used as a loop filter. To determine the two time constants of this loop filter, the parameters of the PLL, ω_n and ξ, need to be determined first according to application. For best suppression of the waiting time jitter, the BW of the PLL must be very narrow. For the experiment described here, the loop filter was designed to give a value for ω_n on the order of $2\pi \times 10$ rad/s. The damping factor ξ was chosen to be 0.707 for initial testing.

Several DPLLs with different BW (10 Hz to 20 Hz) were designed and built for the experimental desynchronizer. Both the waiting time jitter and the acquisition time were measured for these different systems. It was found that a narrower BW suppressed more output phase jitter, but needed a longer acquisition time. Considering these two conflicting properties, we finally chose ω_n to be approximately 82 rad/s (effective BW $\cong$ 13 Hz), which is equivalent to 0.0024 cycles per stuff opportunity. The overall system parameters are:

$K_d \cong 0.08$ V/rad, $K_o \cong 15000$ rad/s-V

$\xi = 0.707$, $\omega_n \cong 82$ rad/s

With $K_o K_d >> \omega_n$, this system is a high-gain loop, so that its phase transfer function can be approximated as Eq. (3.9).

From Eqs. (3.8b) and (3.8c), the time constants may be calculated as:

$$\tau_1 = R_1 C \cong 162 \text{ ms} ,$$

and

$$\tau_2 = R_2 C \cong 16.4 \text{ ms} .$$

The capacitance used has a measured value of $C = 3.42\ \mu F$; therefore, the resistor values are:

$$R_1 = 47.37\ k\Omega ,$$

and

$$R_2 = 4.795\ k\Omega .$$

The standard resistor values of $R_1 = 47\ k\Omega$, and $R_2 = 4.7\ k\Omega$ were chosen in the experiment. Therefore, the real values of τ_1 and τ_2 are equal to 160.7 ms, and 16.1 ms, respectively.

As described in the next section, the measured value of K_o is found to be 15,039 rad/s-V. By substituting

$$\tau_1 \cong 160.7 \text{ ms}, \qquad \tau_2 \cong 16.1 \text{ ms}$$

$$K_d \cong 0.08 \text{ V/rad}, \qquad K_o \cong 15{,}039 \text{ rad/s-V}$$

into Eqs. (3.8b) and (3.8c), the true values of ω_n and ξ can be determined as:

$$\omega_n = \left(\frac{K_o K_d}{\tau_1 + \tau_2} \right)^{1/2} \cong 82.5 \text{ rad/s}$$

$$\xi = \frac{1}{2} \omega_n \left(\tau_2 + \frac{1}{K_o K_d} \right) = 0.698 \cong 0.7$$

For this narrow BW filter, we can expect that this PLL circuit will be suitable for reducing the waiting time jitter on the output clock.

4.3.2.5 Mixer Design

The function of the mixer is to convert the high frequency VCO output to a low frequency signal, so that the digital PLL can operate at the lower bit rate. As the two input signals to the mixer are digital signals, the mixer can be implemented using a phase/frequency detector MC4044, followed by an RC low-pass filter and a Schmitt trigger. The circuit is shown in Figure 4.10. The output of the MC4044, a variable duty cycle signal, has not only the low frequency component of $\Delta f = f_n - f_o$ (approximately 1,800 bits/s), but also some high frequency components (1.544 Mb/s). An RC low-pass filter is necessary in order to filter out (or remove) the high frequency components. As shown in Figure 4.10, the R and C values are chosen to be 1 kΩ and 15 nF, respectively. The corner frequency of this low-pass filter is:

$$\omega_{corner} = \frac{1}{\tau} = \frac{1}{RC} = \frac{1}{1\times10^{3}\times15\times10^{-9}} = 6.67\times10^{4} \text{ rad/s}$$

$$f_{corner} = \frac{\omega_{corner}}{2\pi} = \frac{6.67\times10^{4}}{2\pi} \cong 1.06\times10^{4}\ \text{Hz} = 10.6\ \text{kHz}$$

To convert the low frequency saw-tooth signal to a TTL-compatible logic level, a Schmitt trigger (SN7414) is used. It shapes the waveform so that a clean difference frequency signal at the rate of approximately 1,800 bits/s is generated.

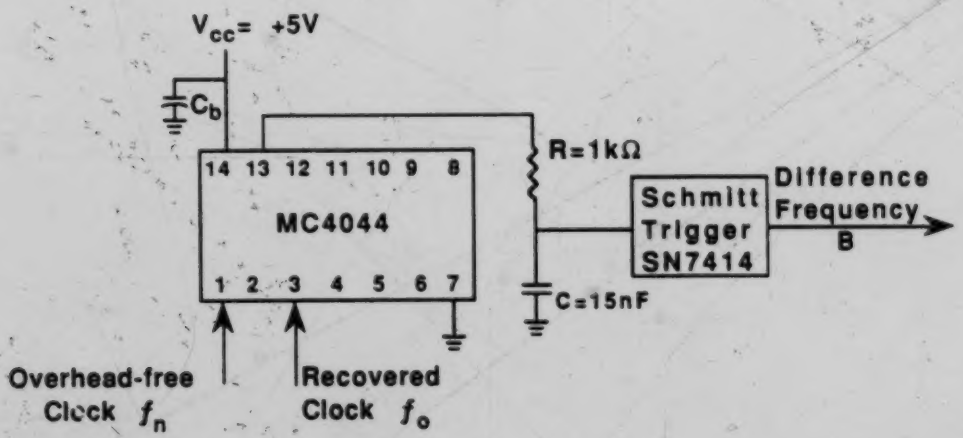


Figure 4.10 Block diagram of the mixer circuit.

4.4 Measuring the DPLL Parameters

For a complete understanding of the circuit performance, it is advantageous to know the real operating parameters of the system. The important parameters, such as K_o, K_d, hold range Δf_H, and lock range Δf_L, are measured in this section. To determine the dynamic response of the DPLL, the acquisition process is captured using a digitizing oscilloscope, and the acquisition time (or the pull-in time) is

measured experimentally.

4.4.1 Measurement of the VCXO Gain

Only the VCXO portion of the DPLL is used for this measurement. Referring to Figure 4.7, we apply a variable DC voltage to pin 2 of the MC4024 as a control voltage. This signal corresponds to the loop filter output signal u_f. By definition, the VCXO gain, K_o, is equal to the variation of VCXO angular frequency $\Delta\omega_o$ in relation to the variation of the u_f signal.

Due to nonlinearity of this VCXO output frequency to the control voltage, the gain value K_o is determined only in the frequency range of ±200 Hz from the centre frequency of 1.544 MHz. The measured data are plotted in Figure 4.11, where it can be seen that the VCXO operates linearly over the desired range. The gain factor is:

$$K_o = \frac{2\pi \times 2.3935 \times 10^3 \text{ rad/s}}{1 \text{ V}} \cong 15039 \text{ rad/s-V}$$

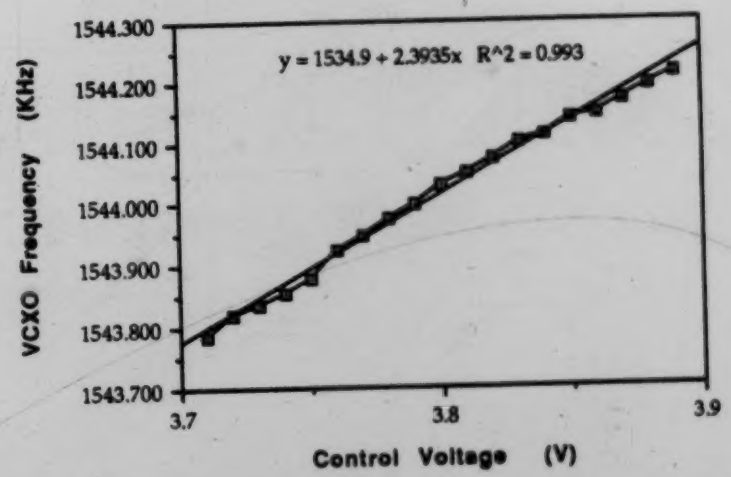


Figure 4.11 VCXO output frequency versus control voltage.

4.4.2 Measurement of the Phase Detector Gain

The test circuit of Figure 4.12 is used for the measurement of K_d. The centre frequency of the VCXO is known to be 1.544 MHz, so that the centre frequency of the mixer output u_2 is approximately 1,800 Hz.

When the frequency of the reference signal u_1 is set to 1,800 Hz, the phase difference of the two input signals of the PD, with u_2 locked to u_1, is measured as $\theta_e = -18.8^\circ \cong -0.328$ radian. For this phase difference, the average (DC) output voltage of the PD, $\bar{u}_d$, is found to be $\bar{u}_d = 4.10$ V. The same procedures are carried out for reference signal frequencies from 1,500 Hz to 2,100 Hz. Both the phase shift and the corresponding average output of the PD are measured. The measured data are plotted in Figure 4.13. From the graph, the phase detector gain factor K_d can be determined as:

$$K_d = \frac{\Delta \bar{u}_d}{\Delta \theta_e} \cong 0.078 \text{ V/rad}$$

It can be seen that the measured value of K_d agrees well with the theoretical value of 0.0796 V/rad, given on page 63.

4.4.3 Measurement of the Hold Range and the Lock Range

There are three important parameters which are used to specify the frequency range of a PLL [31]. They are:

(1) The *hold range* $\Delta\omega_H$: This is the frequency range in which a PLL can statically maintain phase tracking.

(2) The *pull-in range* $\Delta\omega_P$: This is the range within which a PLL will always become locked, provided enough time is allowed for the pull-in

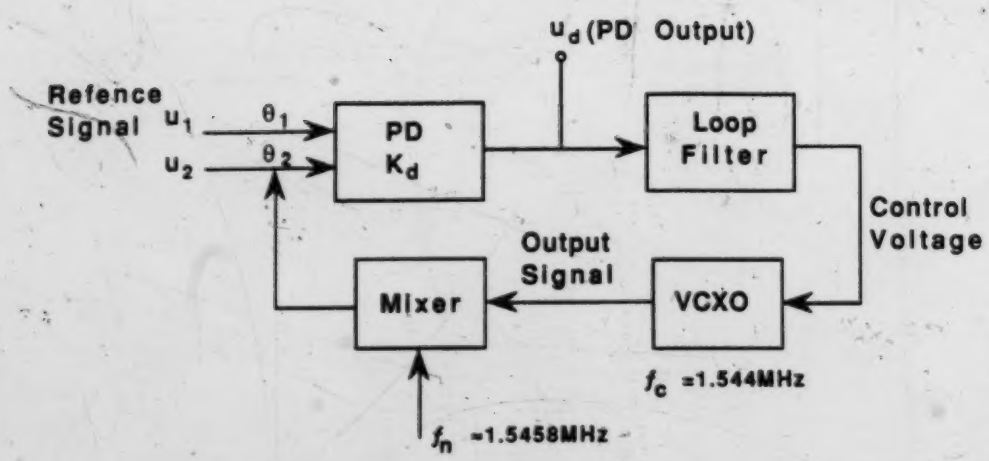


Figure 4.12 Measurement circuit for the PD gain K_d.

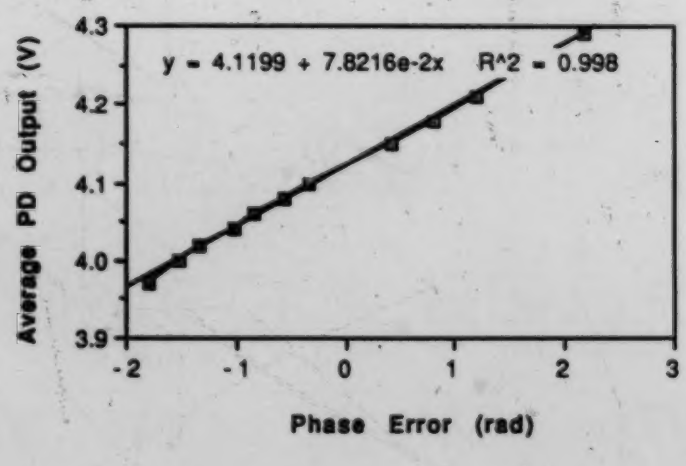


Figure 4.13 Measured PD output voltage $\bar{u}_d$ as a function of phase error θ_e.

process.

(3) The *lock range* $\Delta\omega_L$: This is the frequency range within which a PLL locks within one single-beat note between reference frequency and output frequency. Normally the operating-frequency range of a PLL is restricted to the lock range.

To measure these parameters, the full DPLL circuit must be used (refer to Figure 4.12). A signal generator is applied to the reference input to provide signal u_1. Both the reference signal u_1 and the mixer output u_2 are displayed vs. time on an oscilloscope. The oscilloscope is triggered by the signal u_2.

The frequency of the signal generator is now varied manually until lock-in is observed (Figure 4.14). In case (a), the reference frequency is far away from the centre frequency of about 1,800 Hz, and the system is unlocked. When we change the reference frequency towards the centre frequency, the DPLL starts to pull in the VCXO. As the reference frequency approaches the centre frequency, the DPLL suddenly locks (shown in case (b)). Determination of the hold range Δf_H and the lock range Δf_L is very straightforward. The hold range is measured by slowly varying the reference frequency f_1 and monitoring the upper and lower values of f_1 where the system becomes unlocked. In a similar way, the lock range is determined by monitoring the upper and lower values of f_1 where the system becomes locked. In effect, the value obtained for the lock range in this method yields a value which is between the lock range and the pull-in range. If the reference frequency f_1 is swept very slowly, the measured value comes closer to the pull-in range; if it is swept more quickly, the measured value

comes closer to the lock range. The measured results are listed as follows:

The VCXO centre frequency = 1.544000 MHz ± 10 Hz,

The centre operating frequency of the DPLL ≅ 1,800 Hz.

The hold range:

f_{1max} = 2.895 kHz, f_{1min} = 0.960 kHz

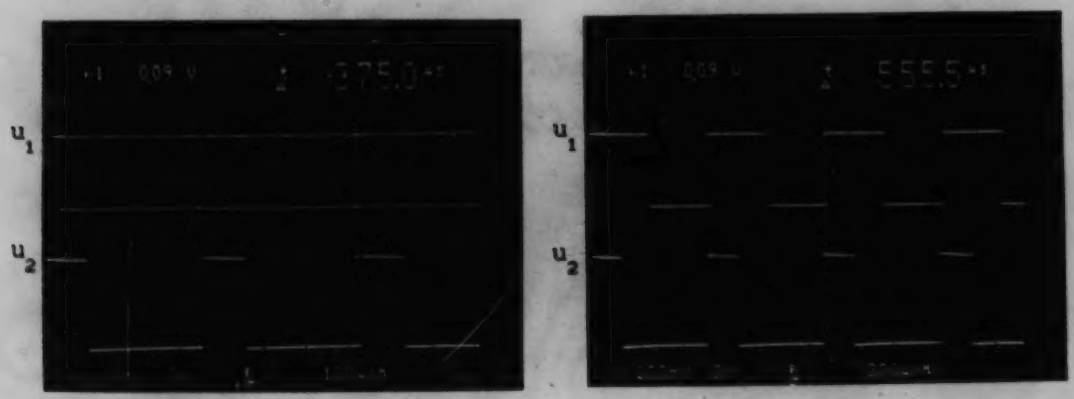
$\Delta f_H = f_{1max} - f_{1min}$ = 2.895 - 0.960 = 1.935 kHz

The lock range:

f_{1max} = 2.630 kHz, f_{1min} = 1.430 kHz

$\Delta f_L = f_{1max} - f_{1min}$ = 2.630 - 1.430 = 1.2 kHz

These DPLL operating ranges are wide enough for clock recovery of DS-1 signals (±200 Hz frequency offsets).



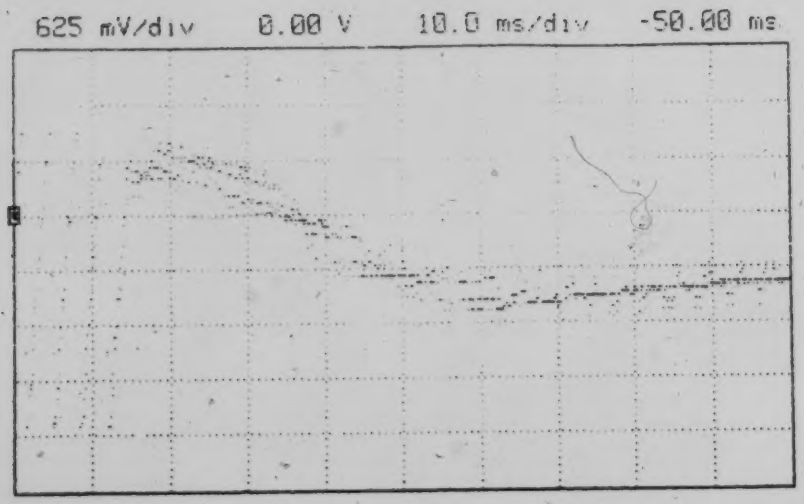
(a) DPLL unlocked (b) DPLL locked

Figure 4.14 Waveforms of signals u_1 and u_2 in the test circuit of Figure 4.12.

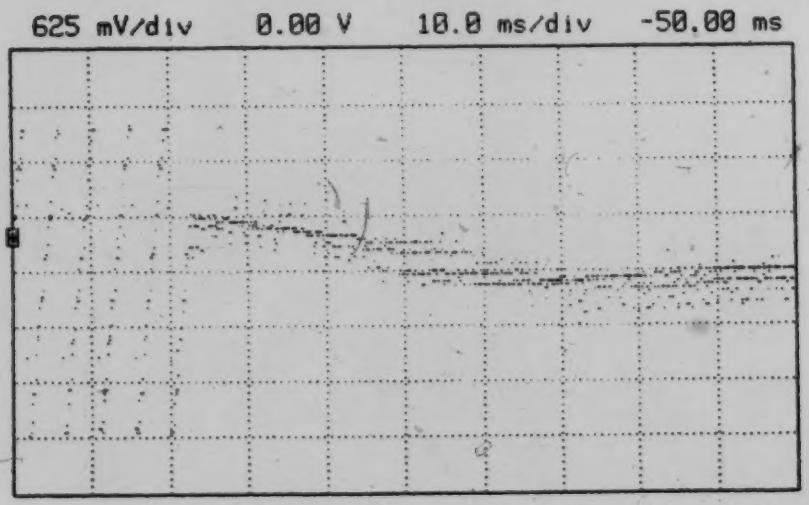
4.4.4 Measurement of the Acquisition Time (Pull-in Time)

If a PLL starts out in an unlocked condition, the process of bringing a loop into lock is called *acquisition*. The "acquisition time" is the time that the PLL takes to achieve the locked state. The acquisition time should be as short as possible, since, during acquisition, the VCO clock timing will be very jittered, and, therefore, some data may be lost. In order to make some estimate of the acquisition time for the proposed DPLL circuit, some measurements have been made using a digitizing oscilloscope (HP 54201A).

The full DPLL circuit is used for this measurement, as shown in Figure 4.5. The digitizing oscilloscope is used to store the PD output. The centre frequency of the VCXO is set to about 1.544000 MHz. Having disconnected the input signal to the DPLL circuit, we observe a saw-tooth waveform on the scope. The DPLL is now in the unlocked state. To observe the pull-in process, the input signal, with a frequency offset $\Delta\omega_o$ from the centre frequency, is connected to the DPLL, and at more or less the same time, the "run/stop" key on the digitizing oscilloscope is pressed. The pull-in (or the lock-in) waveform is thus stored on the scope, and the pull-in time can be estimated. Figure 4.15 shows two typical waveforms for initial offset frequencies of 100 Hz and 200 Hz, respectively. We can see that the pull-in process is almost the same (except for different starting points), and that the pull-in time (until the phase difference reaches the steady state) is approximately 30 ms to 40 ms. The pull-in time varies with the initial frequency offset $\Delta\omega_o$; for smaller $\Delta\omega_o$, the pull-in time will be shorter. For higher frequency offsets, it is



(a) Δf_o = 100 Hz



(b) Δf_o = 200 Hz

Figure 4.15 Pull-in process of the DPLL circuit.

observed that the pull-in process becomes markedly different. Figure 4.16 shows the pull-in process for a frequency offset of 450 Hz. There are several discontinuities in this process; these discontinuities occur when the PD exceeds its linear operating range, and switches from positive to negative output. This slows the pull-in process considerably; at a 450 Hz offset, the acquisition time is about 120 ms. It is evident that the lock-in process occurs very quickly when the input frequency to the DPLL changes within the DS-1 frequency range (0 to 200 Hz).

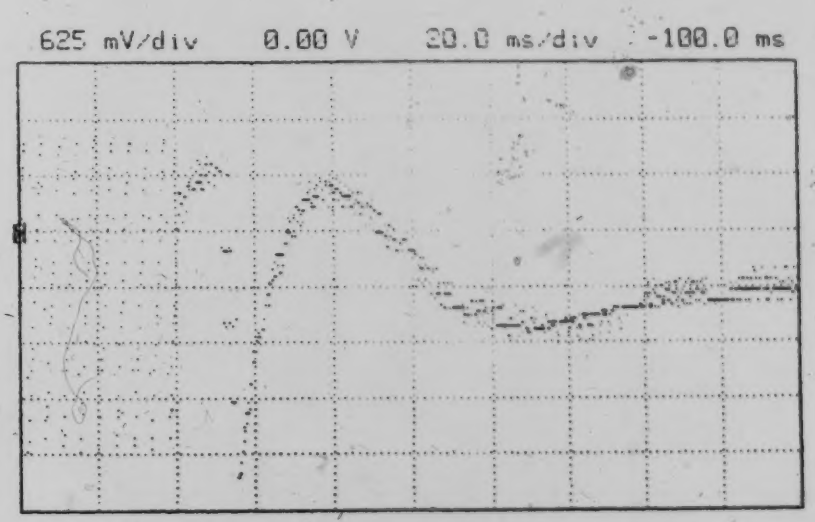


Figure 4.16 Pull-in process for Δf_o = 450 Hz.

Summary

In this chapter, a new desynchronizer for reducing waiting time jitter in digital TDM systems has been proposed. The circuit has been described and implemented experimentally for an M12 system. The most important part of the new desynchronizer, the DPLL clock recovery

circuit, has been carefully designed, and the important DPLL parameters have been measured. In the next chapter, the measured waiting time jitter results for the experimental system will be presented and discussed. Waiting time jitter spectra will also be analyzed.

CHAPTER 5
EXPERIMENTAL WAITING TIME JITTER RESULTS AND DISCUSSION

In this chapter, the results obtained for the experimental desynchronizer, as discussed in the previous chapters, are given. The circuitry used to measure the amount of waiting time jitter present on the recovered clock is described. Time domain measurements are made using a digitizing oscilloscope; estimates of the peak-to-peak and rms jitter, as well as some typical jitter waveforms are presented. Frequency domain measurements are also made in order to determine the spectral characteristics of the waiting time jitter. Finally, the results for the new clock recovery circuit are discussed, and some comparisons are made with presently-used desynchronizers.

5.1 Basic Principles

Waiting time jitter is a slowly changing time difference between the recovered clock and the original clock. The waiting time jitter present on the recovered clock (for the experimental M12 system) can be observed on an oscilloscope. Figure 5.1 shows the original clock (top trace), and the recovered clock (lower trace). Both clocks have the same average bit rate. With the oscilloscope triggered by the original clock, the jitter on the recovered clock causes blurring of the rising and falling edges of the output clock signal. The amount of peak-to-peak jitter can be estimated by the width of the blurred edges of the recovered clock.

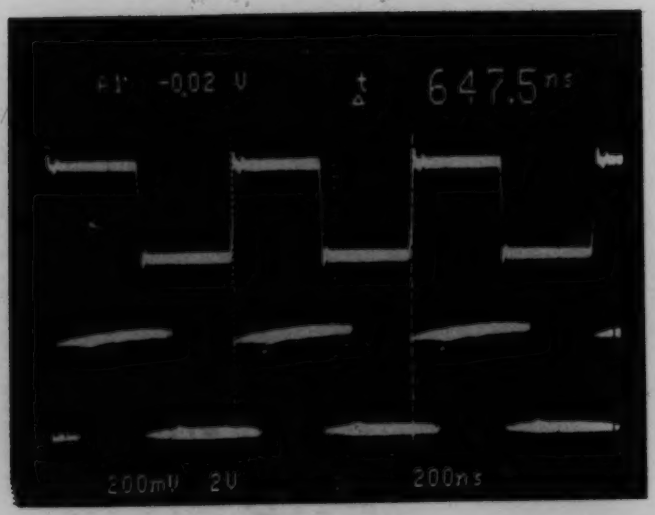


Figure 5.1 The original DS-1 clock and the recovered clock of the improved desynchronizer (f = 1.544000 MHz).

In order to make accurate measurements and obtain the jitter spectrum, a circuit needs to be built to convert the phase differences (i.e. phase jitter) between the recovered DS-1 clock and the original DS-1 clock into a voltage waveform. The characteristics of the waiting time jitter can then be analyzed through this voltage waveform, and be presented in either the time domain or the frequency domain using the following steps:

(1) Sampling the voltage waveform (i.e. waiting time jitter signal), and storing these samples in a sufficiently large memory. Application of time domain signal processing to the phase difference samples to calculate the rms and the peak-to-peak waiting time jitter for the different input frequency offsets over the allowed DS-1 frequency range (±200 Hz).

(2) Frequency domain analyses of the voltage waveform to obtain the spectral components of the waiting time jitter.

5.2 Waiting Time Jitter Measurements

In order to estimate the waiting time jitter present on the recovered data in the time domain and in the frequency domain, jitter measurement and analysis need to be carried out. An HP5785 Jitter Test Set can be used for this purpose. Because this instrument is not available in our laboratory, a jitter measurement device had to be constructed. Figure 5.2 illustrates the test configuration for the waiting time jitter measurement and analysis.

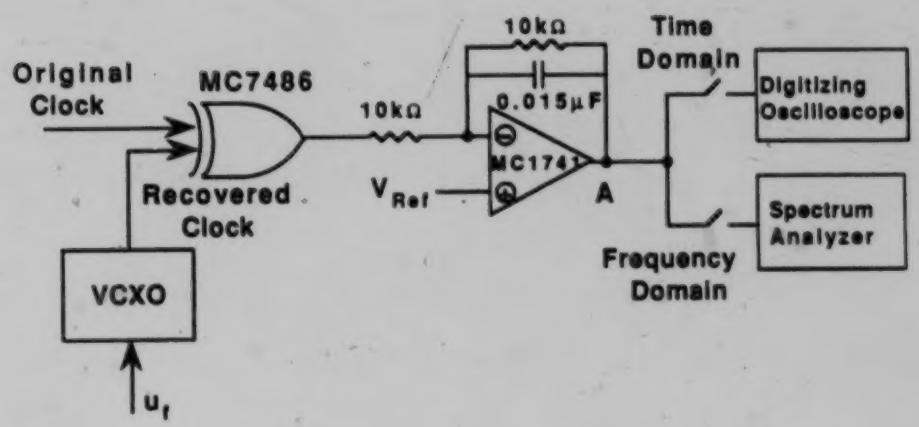


Figure 5.2 Waiting time jitter measurement configuration.

The measurement circuit consists of an EX-OR gate followed by a low-pass filter. The recovered DS-1 clock and the original DS-1 clock form the two inputs to the EX-OR gate. The output of the EX-OR is high

only when its two inputs differ, so that the average output voltage will be proportional to the amount of time difference of the two clock signals. Thus, the average output voltage can be used to measure the phase jitter between the original clock and the recovered clock. The active low-pass filter must pass all the jitter frequency components, but remove the DS-1 rate components from the EX-OR gate output. Because frequency components of the waiting time jitter usually extend from 10 Hz to 1 kHz, and components for high frequencies are typically reduced to a negligible level by the desynchronizer PLL response [30], the 3 dB cutoff frequency of this low pass filter was set to approximately 1 kHz. A reference voltage V_{Ref} was applied to the positive input terminal of the op amp (MC1741) to cancel the DC voltage offset, which resulted from the constant component of the phase difference between the two inputs to the EX-OR gate (somewhere close to 90° phase shift). Therefore, the jitter information was converted to an analog voltage, appearing at the output of the low-pass filter. To carry out time domain analysis, an HP 54201A digitizing oscilloscope [32] was used to store the jitter waveforms and sample them over a typical period of several hundred milliseconds. The peak-to-peak and the rms jitter values were then estimated from these samples. For frequency analysis of the jitter components, a Systron-Donner Model 710/800 Spectrum Analyzer was used to display the spectrum.

5.3 Waiting Time Jitter Analysis in the Time Domain

The waiting time jitter, for the new M12 desynchronizer circuit,

was measured over the full DS-1 frequency offset range of 0 to 200 Hz. The peak-to-peak and the rms jitter of the recovered clock were obtained using the measurement circuit described in Section 5.2, followed by the HP 54201A digitizing oscilloscope. The measurement setup converts the output clock jitter to an analog voltage, and samples of the output voltage are stored and analyzed using the digitizing oscilloscope. If the voltage samples are denoted by u(k), an estimation of the rms and of the peak-to-peak of this voltage waveform are given by the standard deviation and peak excursion of the voltage samples as:

$$u_{rms} = \sqrt{\frac{1}{N}\sum_{k=1}^{N}\left(u(k) - u_{mean} \right)^2}$$

$$= \sqrt{\frac{1}{N}\sum_{k=1}^{N}\left(u(k) \right)^2 - \left(\frac{1}{N}\sum_{k=1}^{N} u(k) \right)^2} \qquad (6.1)$$

and

$$u_{p-p} = \max u(k) - \min u(k) \qquad k = 1, 2, \cdots, N \qquad (6.2)$$

In order to convert the output voltage measurement to a waiting time jitter estimation, i.e.

$$\theta_{rms} = K u_{rms} ,$$

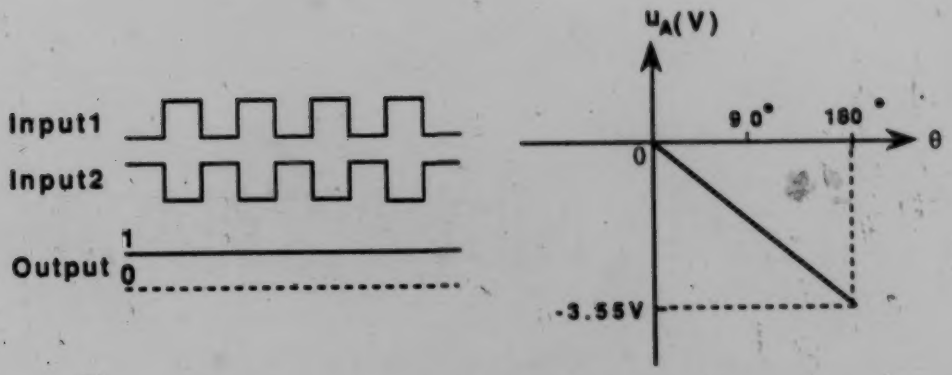
and

$$\theta_{p-p} = K u_{p-p} ,$$

the constant K must be determined experimentally. If the two input signals to the EX-OR gate are phase shifted by 180°, as shown in

Figure 5.3a, the output of the EX-OR stays "high". Measuring the DC voltage at point A of Figure 5.2 (with V_{Ref} = 0), we obtained u_A = -3.55 V. It can be seen from Figure 5.3a that the phase difference of these two signals now reaches 0.5 UI of the Input 1. The linear relation between the output voltage u_A and the phase differences of the two inputs θ is shown in Figure 5.3b. The constant K is, therefore, determined as:

$$K = \frac{0.5\ UI}{3.55\ V} = 0.14\ UI/V$$



(a) EX-OR output for two inputs with 180° phase difference

(b) The output voltage u_A versus the phase differences of the two inputs θ

Figure 5.3 Conversion of phase difference to output voltage.

Therefore, the rms and the peak-to-peak jitter can be estimated by:

$$\theta_{rms} = 0.14\ u_{rms}\ , \tag{6.3}$$

and

$$\theta_{p-p} = 0.14\ u_{p-p}\ . \tag{6.4}$$

There is an important consideration in the measurement, the *sampling duration*, which is the amount of real-time over which the voltage samples are stored to produce the rms and the peak-to-peak jitter estimates. The sampling duration required to produce accurate measurement results depends on the frequency components contained within the jitter spectrum. To obtain an accurate estimate of the jitter components, the sample length should extend at least over several cycles of the lowest frequency component. In general, a sampling duration of 1 second is sufficient for most values of stuff ratio. If inherently low frequency components are present, as in the case where the stuff ratio is close to a simple fraction such as 1/3, the sampling duration must be longer in order to produce accurate results [30]. For the measurements reported in this thesis, a sampling duration of 1 second was used for most offsets. For offsets ranging from 0 to 12 Hz, a sampling duration of 2 seconds was used, with the exception of 7 Hz, where a sampling duration of 5 seconds was employed.

The experimental results of the peak-to-peak and the rms jitter for the new desynchronizer are shown in Figure 5.4 [33]. The measured maximum peak-to-peak jitter value is approximately 0.33 to 0.34 UI, occurring at a DS-1 offset frequency near 7 Hz. This offset

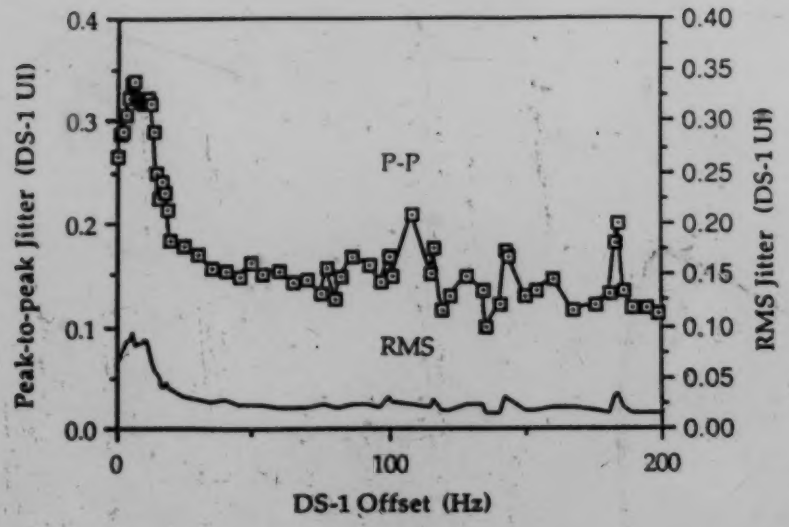


Figure 5.4 Peak-to-peak and rms jitter versus DS-1 offset frequency.

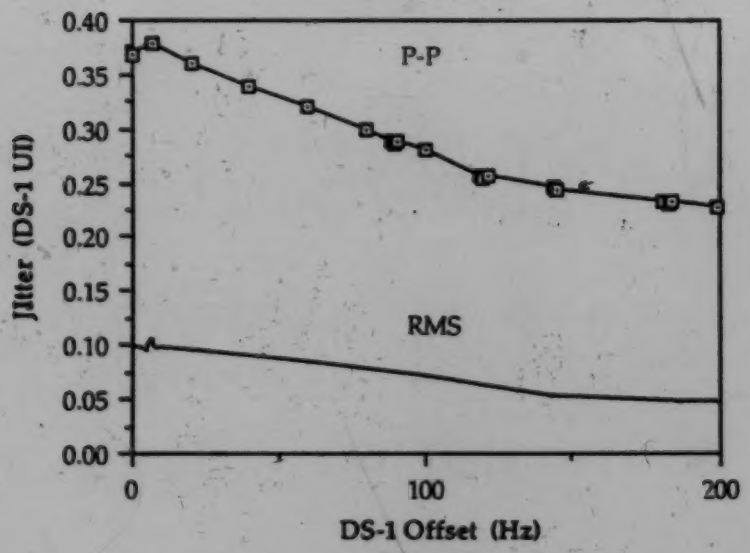


Figure 5.5 Computer-simulated peak-to-peak and rms jitter versus DS-1 offset frequency. (From Ref.[30])

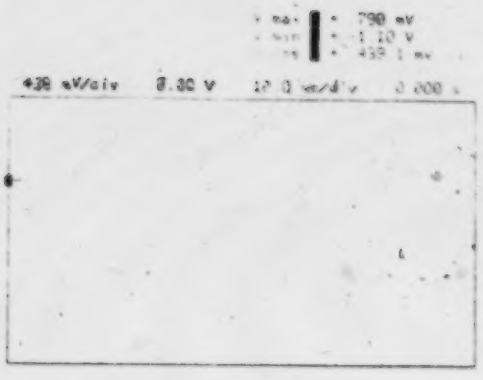
corresponds to a stuff ratio close to one-third ($\rho \cong 0.333$), where the theoretical peak-to-peak jitter is expected to be 0.33 UI. The rms jitter for this particular stuff ratio is measured to be approximately 0.09 UI. Apart from this critical stuff ratio, the waiting time jitter is quite small, typically about 0.1 UI, with an rms jitter of about 0.02 UI. The maximum rms jitter occurs at the same offset as the maximum peak-to-peak jitter. For comparison with the presently-used method, we also reproduce in Figure 5.5 the typical peak-to-peak and rms jitter of a conventional M12 clock recovery system using a standard PLL circuit at 1.544 Mb/s (BW ≅ 350 Hz), obtained by T.E.Moore, *et al* [30] using computer simulation. Comparing these results, it can be seen that the proposed new desynchronizer suppresses the waiting time jitter by approximately 50% over most of the DS-1 frequency range.

Several different output voltage waveforms (i.e. the waiting time jitter signals) for several different stuff ratios (or offset frequencies) are shown in Figure 5.6. Figure 5.6a shows the jitter waveform for the offset frequency of 0 Hz ($\rho \cong 0.3346$). Figure 5.6b is for the worst jitter case with the offset frequency of 7 Hz ($\rho \cong 0.333$). Figure 5.6d is typical for stuff ratios which are well away from the critical value of one-third.

5.4 Waiting Time Jitter Observation in the Frequency Domain

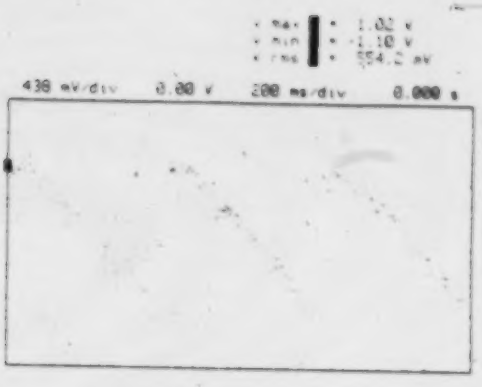
The waiting time jitter spectrum can be obtained in two ways:

(1) FFT method: Using the stored voltage samples obtained as described in Section 5.3, a computer can be used to obtain and plot a sample



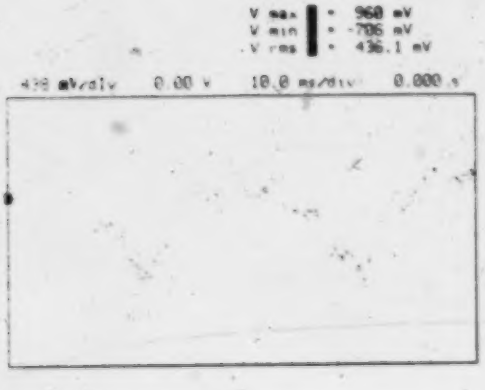
(a) Offset frequency = 0 Hz

(ρ ≅ 0.3346)



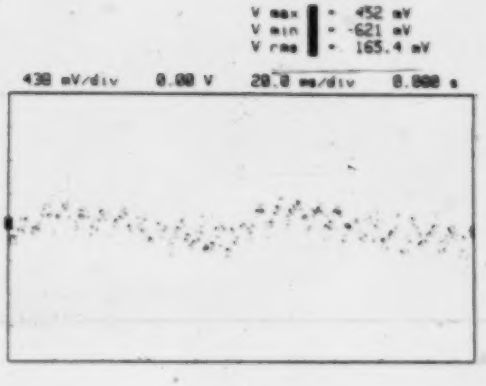
(b) Offset frequency = 7 Hz

(ρ ≅ 0.3333)



(c) Offset frequency = 13 Hz

(ρ ≅ 0.3322)



(d) Offset frequency = 100 Hz

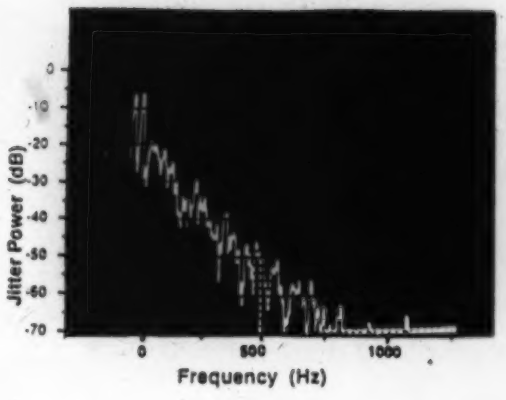
(ρ ≅ 0.3160)

Figure 5.6 Typical waiting time jitter signals.

spectrum using the Fast Fourier Transform (FFT).

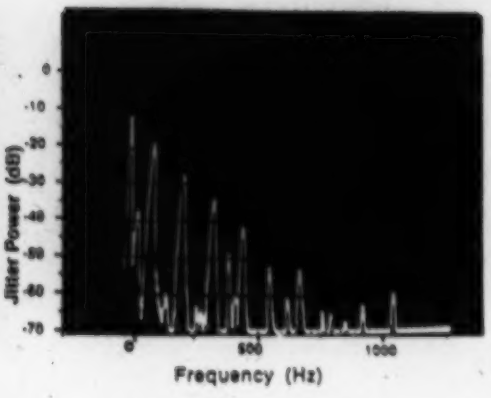
(2) Direct method using a spectrum analyzer: To perform a waveform analysis, a spectrum analyzer can be used to display the spectrum directly. For waiting time jitter frequency analysis, the spectrum analyzer should have good sensitivity and resolution down to very low frequencies (≈ 10 Hz). A Systron-Donner Model 710/800 Spectrum Analyzer was employed to obtain the waiting time jitter spectrum. The frequency components of interest are in the range 10 Hz to 1 kHz. The frequency components above 1 kHz are quite small. The centre frequency of the spectrum analyzer is set to 500 Hz. The scan width is 150 Hz/cm (10 cm in total), and the sweep time is 0.3 s/cm (i.e. every 3 seconds the spectrum analyzer is swept). Figure 5.7 shows several typical spectra of the jitter for different input frequency offsets. Although the vertical scale does not correspond to any particular amount of jitter power, it shows the relative amplitudes of the different frequency components. We observe that only the very low frequency components (≤ 500 Hz) of the waiting time jitter cannot be adequately filtered, and that the higher frequency components are typically reduced to a very low level. For example, for frequency of 500 Hz, the jitter component is about 30 dB down, and for frequency of 1 kHz, the jitter is typically about 40 dB down. The jitter components above 1 kHz are thus reduced to a negligible level. The area under the jitter spectral curve is proportional to the jitter power which, neglecting the DC offset, is equal to the jitter variance.

Figure 5.7 clearly shows the effect of the narrow PLL bandwidth on the waiting time jitter spectrum. If the jitter spectrum contains



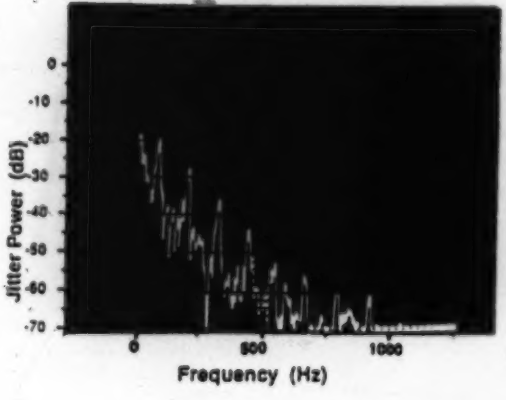
(a) Offset frequency = 0 Hz

(ρ = 0.3346)



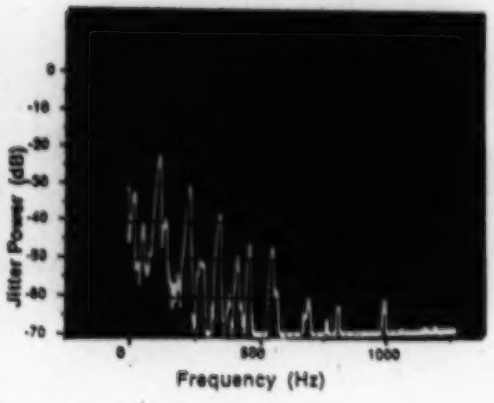
(b) Offset frequency = 7 Hz

(ρ = 0.3333)



(c) Offset frequency = 13 Hz

(ρ = 0.3322)



(d) Offset frequency = 100 Hz

(ρ = 0.3160)

Figure 5.7 Typical waiting time jitter spectra.

more low frequency components (extending to DC), such as for $\rho \approx 1/3$, these low frequency components cannot be removed by the PLL, even when a very narrow filter BW is used. Then, the jitter reduction is not significant, as shown in Figure 5.7b. For other stuff ratios, the frequency components are at higher frequencies, and so are greatly attenuated by the PLL filter. For low frequencies, the jitter components are typically about 10 dB less than the worst case, as shown in Figure 5.7d. We can thus expect that the jitter is about 1/3 of the worst case value. This is supported by the time domain measurements. Overall, the results indicate that the waiting time jitter can be greatly reduced over most of the DS-1 frequency range (for an M12 system).

CHAPTER 6
SUMMARY AND CONCLUSION

The pulse stuffing synchronization method for time division multiplexed systems has been presented and discussed. The pulse stuffing mechanism is seen to be the source of a very low frequency noise impairment, waiting time jitter, whose accumulation results in detrimental effects on the performance of telecommunication systems. This thesis has studied waiting time jitter, and investigated a new technique by which waiting time jitter can be considerably reduced, as compared to the presently-used method.

A new desynchronizer (or clock recovery circuit) for reducing waiting time jitter in digital TDM systems has been described. This circuit makes use of the irregular stuff pulses to control the PLL clock recovery circuit. Since the PLL operates at a much lower frequency, a very narrow BW filter can be readily achieved, which will, in general, reduce the amount of waiting time jitter present on the recovered clock. To test the jitter performance of the new desynchronizer, an experimental system for the M12 format has been set up and tested. The most important part of the new desynchronizer, the DPLL circuit has been designed using simple circuitry, with narrow BW, high gain and quick acquisition process (lock-in time is less than 50 ms).

The waiting time jitter of the recovered DS-1 clock for the improved desynchronizer has been measured and analyzed in the time domain and in the frequency domain. Initial experimental results indicate that this new method of clock recovery can result in a

significant reduction (approximately 50% for most DS-1 frequency offsets in an M12 system) in both the peak-to-peak and the rms waiting time jitter, as compared to the presently-used method.

Although we have experimentally implemented the proposed new desynchronizer for an M12 system, and have shown that it can offer a significant improvement in performance as compared to clock recovery circuits using the usual PLL, there are several interesting areas of research that need to be investigated. Circuit optimization can be carried out in order to further improve the performance of the proposed desynchronizer. An active loop filter, which theoretically has a better filtering effect, can be used, and an optimized VCXO can be designed. For the phase detector, faster counters and a faster op-amp circuit can be used to extend its response speed to higher frequencies, so that the new desynchronizer circuit could be used in M23 (DS-2 to DS-3) and M34 (DS-3 to DS-4) systems. A mathematical analysis or a computer simulation of the circuit operation would be very useful for not only prediction of the waiting time jitter, but also determination of the pull-in and lock-in processes. A comparison could then be made with the measured results. The computer simulation can also be extended readily to other digital multiplexers, such as M23 and M34; in this way, the reduction of the waiting time jitter could be predicted, without experimental circuit implementation being required.

It is hoped that the work in this thesis will lay the foundation for future work on waiting time jitter reduction in digital telecommunication networks. A future interesting research direction is

to study waiting time jitter in the Synchronous Optical Network (SONET), and to consider the use of the proposed desynchronization method in relation to SONET.

SONET, a digital signal hierarchy of the rates and formats for optical interfaces [34, 35], is currently being standardized by the Exchange Carriers Standards Association (ECSA) and the International Telegraph and Telephone Consultative Committee (CCITT). The purpose of the SONET standard is to establish an optical interface specification with sufficient flexibility to transport many different payloads (i.e. voice, data, video, and new services). In addition, the standard for SONET must try to resolve the incompatibilities between the European signal hierarchy (based on 2.048 Mb/s) and the North American signal hierarchy (based on 1.544 Mb/s), so that it becomes an international transmission standard [35].

Synchronization in SONET is handled using methods similar to those used in today's networks. For timing recovery of plesiochronous payloads, destuffing, followed by PLL smoothing of the gapped clock is used. Therefore, transport of plesiochronous signals (such as DS-1 and DS-3) in SONET must again result in a waiting time jitter impairment. When the traditional pulse stuffing synchronization technique is applied to SONET, as a means of providing the desired plesiochronous compatibility, an unacceptably high waiting time jitter is introduced. This is because the "proposed synchronous standards" work at a low pulse stuffing frequency ($\rho \approx 0$), which gives rise to high-amplitude low-frequency jitter components, which are not easily attenuated by a PLL. Some research [36, 37, 38] has been carried out to study the

waiting time jitter performance and its reduction in SONET.

As a future study, the principle of the differential PLL desynchronizer could be considered as a possible means of reducing jitter in SONET. It may be that a computer could be used to average the stuff pulses over a longer period of time, and to set the VCO frequency to the "exact" average bit rate of the input signal.

APPENDIX I

THE PULL-IN PROCESS FOR A DIGITAL PLL

To compare the time constant of the pull-in process of the new DPLL circuit and the conventional PLL, we assume a type-4 phase/frequency detector (such as the MC4044) as a PD, an active filter (shown in Figure 3.7b) as a loop filter. A linear model has been established for analyzing the pull-in process of the digital PLL, and the time constant of the pull-in process can be calculated by [39]:

$$T_P = \tau_2 + \frac{\tau_1}{K_o K_d'} ,$$

where K_d' (V-s/rad) is the phase detector gain in the unlocked state, and

$$K_d' \cong \frac{U_B}{\omega_0}$$

U_B is the output-high voltage of the PD , and ω_0 is the center frequency of the PLL related to its inputs.

Here a numerical example is presented. The DPLL circuit operates at the stuffing rate of about 1,800 bits/s, therefore, the K_d' is:

$$K_d' \cong \frac{U_B}{\omega_o} \cong \frac{3.5}{2\pi \times 1800} \cong 0.309 \times 10^{-3} \text{ V-s/rad}$$

By using the data given in Section 4.3.2.4, namely:

$\tau_1 \cong 160$ ms ,

$\tau_2 \cong 16$ ms ,

$K_o \cong 15000$ rad/s-V ,

the pull-in time constant can be estimated as:

$$T_P = \tau_2 + \frac{\tau_1}{K_o K_d'} = 16 + \frac{160}{15000 \times 0.309 \times 10^{-3}} \cong 50.5 \text{ ms}$$

If the PLL synchronizes directly with the gapped clock at the bit rate of 1.544 Mb/s, then K_d' is much smaller, and

$$K_d' \cong \frac{U_B}{\omega_o} \cong \frac{3.5}{2\pi \times 1.544 \times 10^6} \cong 0.361 \times 10^{-6} \text{ V-s/rad}$$

Therefore,

$$T_P = \tau_2 + \frac{\tau_1}{K_o K_d'} \cong 16 + \frac{160}{15000 \times 0.361 \times 10^{-6}} \cong 29581.7 \text{ ms} \cong 29.6 \text{ s}$$

Compared with the result of the improved DPLL circuit, this pull-in time constant is much longer. Therefore, the low operating frequency of the DPLL speeds up the pull-in process of the narrowband loop.

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